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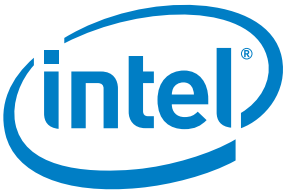

Intel® PON Chipset
Intel® 10G PON Chipset

EASY 98900

SFP Base Board V2.2

for

Intel® PON Chipset PEB/PEF 98035 ET, V1.3
Intel® PON Chipset PEB/PEF 98036 ET, V1.3
Intel® 10G PON Chipset PRX126
EASY 98035 SFP Reference Stick V1.2/V1.3
EASY 98035-1588 SFP Reference Stick V1.2/V1.3
EASY 98036 SFP Reference Stick V1.2
Intel® 10G PON Development Kit EASY PRX126 EVAL BOARD

Hardware Description

Intel Confidential

Revision 1.0, 2020-04-23
Reference ID 619058

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Revision History

Current:	**Revision 1.0, 2020-04-23**
Previous:	**None**

Page	Major changes since previous revision

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Preface

This document describes the basic structure and features of the EASY 98900 SFP Base Board V2.2 (SFP Base Board).

The SFP Base Board is designed for use with several different SFP/SFP+ Modules with Intel® PON Chipset and Intel® 10G PON Chipset devices:

- EASY 98035 SFP Reference Stick V1.2/V1.3
- EASY 98035-1588 SFP Reference Stick V1.2/V1.3
- EASY 98036 SFP Reference Stick V1.2
- Intel® 10G PON Development Kit EASY PRX126 REF BOARD

To simplify matters, the following synonyms are used:

PEB/PEF 98035 ET

Synonym used to refer to the Intel® PON Chipset PEB 98035 ET/PEF 98035 ET, V1.3 device.

SFP Module

Synonym used to refer to the following SFP Modules with Intel® PON Chipset PEB/PEF 98035 ET or PEB/PEF 98036 ET:

- EASY 98035 SFP Reference Stick V1.2/V1.3
- EASY 98035-1588 SFP Reference Stick V1.2/V1.3
- EASY 98036 SFP Reference Stick V1.2

SFP+ Module

Synonym used to refer to the following SFP+ Module with Intel® 10G PON Chipset PRX126 device:

- Intel® 10G PON Development Kit EASY PRX126 REF BOARD

SFP/SFP+ Module

Synonym used to refer to both the Intel® 10G PON Development Kit EASY PRX126 REF BOARD and the EASY 98035/EASY 98036 SFP Reference Sticks.

SFP Base Board

Synonym used to refer to the EASY 98900 SFP Base Board V2.2.

Organization of this Document

- **Chapter 1, Overview**
  Overview of the features of the SFP Base Board, including a block diagram.
- **Chapter 2, Interfaces and Pinout**
  Description of the interfaces of the SFP Base Board.
- **Chapter 3, SFP Base Board Control**
  Description of SFP Base Board mode control.
- **Chapter 4, SFP Base Board Configuration**
  Description of SFP Base Board configuration.
- **Literature References**
- **Terminology**

1 Overview

The SFP Base Board allows the SFP/SFP+ Module for 1G, 2.5G, 5G and 10G speeds to be operated via a standard SFP interface. It is implemented as a 4-layer PCB and offers the following operating modes:

- Programming the SFP/SFP+ Module and downloading software onto the on-board flash memory.
- Demonstrating SFP/SFP+ Module operation.

The SFP/SFP+ Module (with metal housing) is plugged into the metal cage with the connector socket on the SFP Base Board, as shown in **Figure 1**.

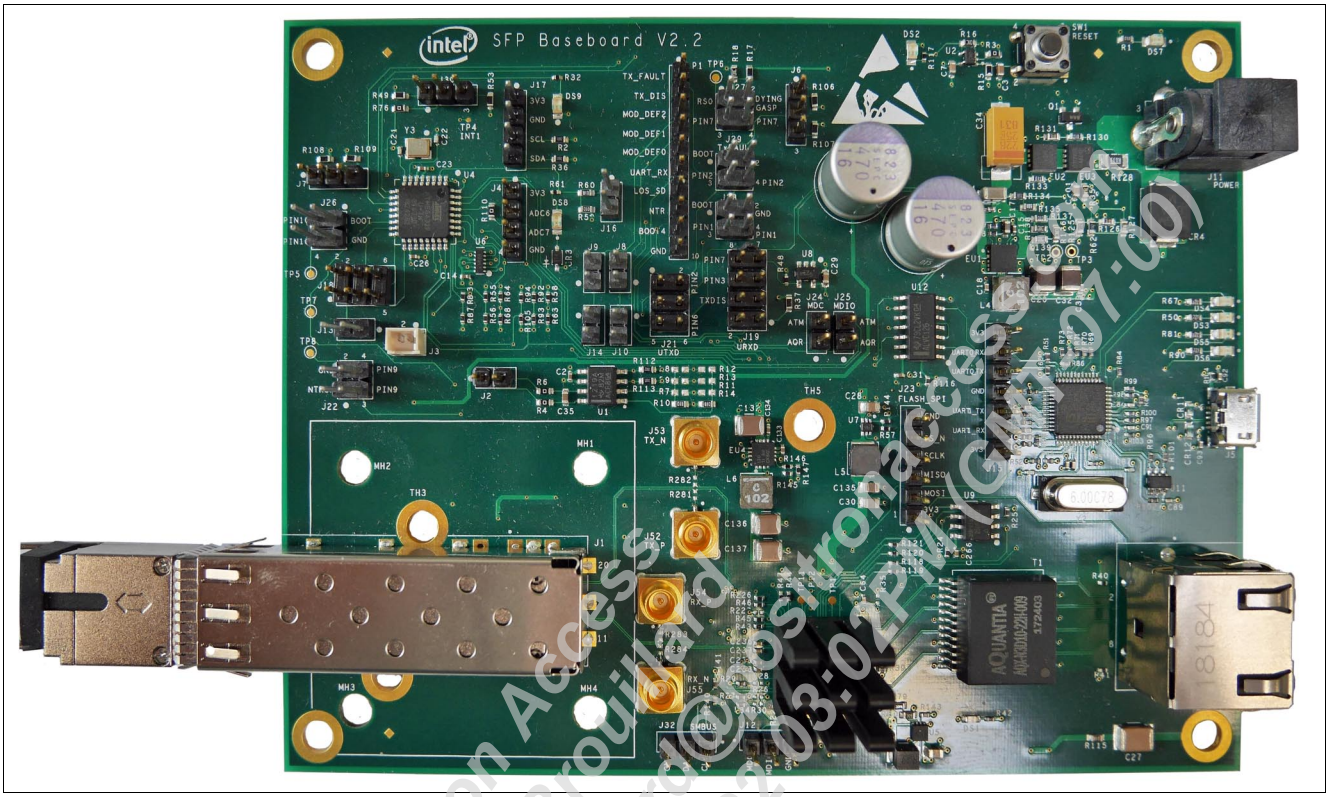

Figure 1 SFP/SFP+ Module (in Metal Housing) Plugged into Metal Cage on SFP Base Board

1.1 Block Diagram

As shown in **Figure 2**, the SFP Base Board consists of the following blocks:

- SFP Module connector where SFP/SFP+ Module is plugged in
- Aquantia* PHY AQR107
- Atmel* ATMega328 processor
- USB connector supports 2 x UART interface via FTDI chip
- UART interface for Atmel* ATMega328 processor
- UART interface for SFP/SFP+ Module connector
- I^2C current measurement device
- DC/DC converter: +12 V to +3.3 V
- DC/DC converter for Aquantia* PHY

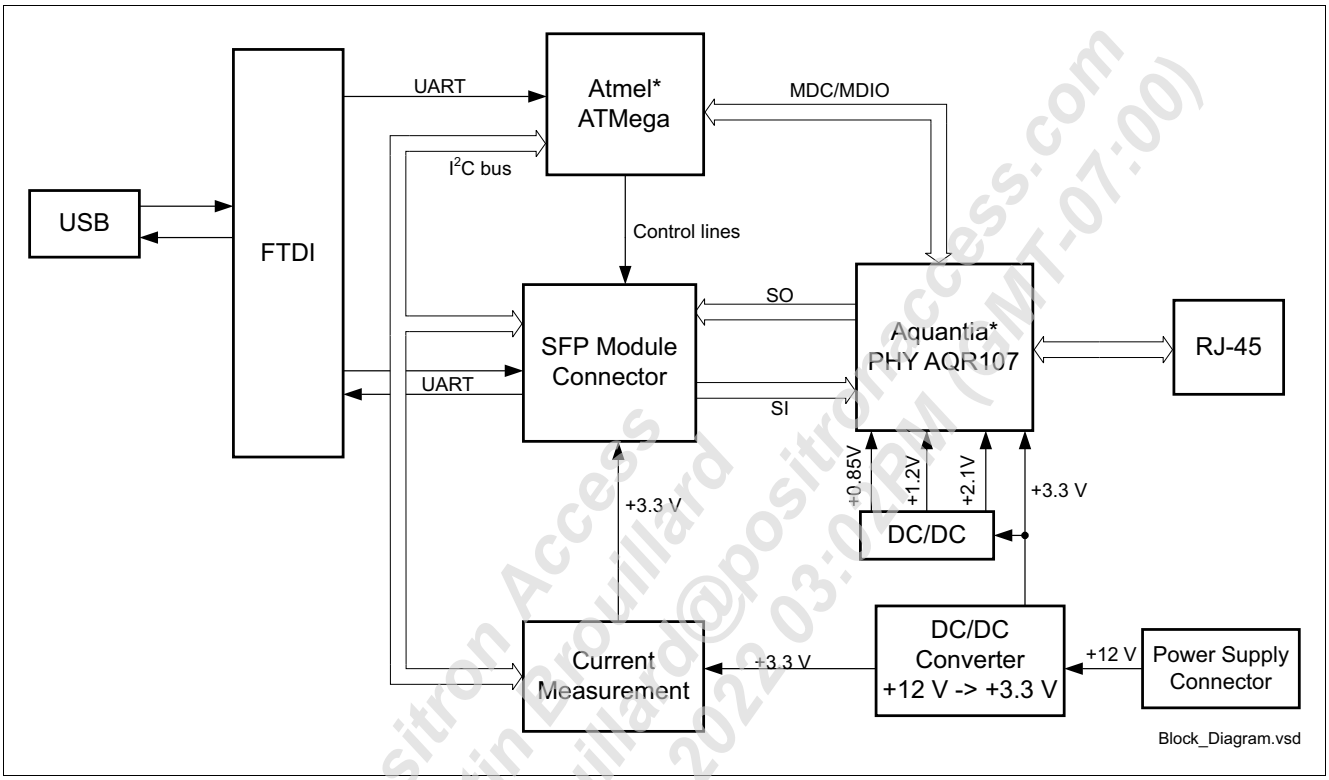

Figure 2 Block Diagram of SFP Base Board

1.2 SFP Module Connector

A standard SFP cage is mounted on the SFP Base Board and any SFP/SFP+ Module that is equipped with the standard interface can be plugged onto the SFP Base Board. A number of resistors and jumpers around the connector are used to rearrange the connector pinout so that modules with different pinouts can be used. The SFP/SFP+ Module is powered with +3.3 V via this connector.

The I^2C bus on the SFP Base Board is connected to the SFP Module connector and allows access to the SFP/SFP+ Module memory. The internal registers of the SFP/SFP+ Module can be configured via this I^2C interface. A number of the pins on the SFP/SFP+ Module can have multiple functions. The function of each pin is described in **Chapter 2.1**.

For software development purposes, the SFP Module connector pinout can be modified using jumpers to set different boot modes for the PEB/PEF 98035 ET, PEB/PEF 98036 ET and PRX126 devices. The standard MSA specification uses pins 1 and 10 as GND pins. These pins are also used to select Intel-specific boot mode options, which allow firmware to be downloaded onto the SFP/SFP+ Module via the UART or SGMII interface (described in **Chapter 4.1.2**). When the UART interface is selected, two of the connector pins (1, 3 and 6, 7) are used for the serial interface (refer to **Table 13**). The functions of other pins on the SFP Module connector can also be modified (refer to **Chapter 4.3** and **Chapter 4.4**).

Data is transferred between the SFP/SFP+ Module and the Aquantia* PHY AQR107 device via the SGMII or XFI interface.

1.3 Aquantia* PHY AQR107

The Aquantia* PHY AQR107 device is used to transfer data via XFI from the SFP/SFP+ Module to the 1, 2.5, 5 or 10 Gigabit Ethernet interface (RJ-45) and vice versa. The AQR107 is controlled by the ATMega328 processor via the MDIO interface and is powered from the SFP Base Board power supply. A crystal is connected to the AQR107 device for clock generation.

1.4 ATMega328 Processor

The Atmel* ATMega328 processor is the control instance used to interface a PC with the SFP/SFP+ Module and the Aquantia* PHY AQR107 device via the MDIO/MDC. Data from the PC can be transferred to the SFP Base Board via the USB interface using a command line interface. All the commands sent from the PC are interpreted by the processor and transfered via the I^2C bus to the SFP/SFP+ Module or via the MDC/MDIO to the Aquantia* PHY AQR107. In the opposite direction, the information from the SFP/SFP+ Module is transferred to the PC via the USB interface. The direction and value of GPIOs can be set some changes in the GPIO values interpreted.

A current sensor on the SFP Base Board is used to measure the power supply current consumed by the SFP/SFP+ Module. This device is also connected to the I^2C bus and uses a different address to that of the SFP/SFP+ Module. The additional control lines of the SFP Module connector can also be controlled by the ATMega328 processor.

1.5 USB Interface Connector

The SFP Base Board is connected to a PC via the FTDI device to the USB interface. This is a Version 2.0 interface, but is also compatible with Version 1.0. The two on-board UARTs, one from the ATMega328 and the other from the SFP/SFP+ Module and both are connected to the FTDI, which handles both interfaces via one USB interface.

The self-powered mode of the USB interface is not used. The SFP Base Board is powered by an external power supply.

1.6 UART Interfaces

The SFP Base Board has two UART interfaces. The first operates with 57600 Baud, 1 stop bit and 8 data bits (XON/XOFF is not supported). The second operates with 115200 Baud, 1 stop bit and 8 data bits (XON/OFF is not supported). They are provided by the FTDI device.

One interface is connected to the ATMega328 processor for system control and the retrieval of system status information. The second UART interface is connected to the SFP/SFP+ Module for debugging purposes. There are jumpers for each of the both UARTs, which allows the configuration of the connections.

The UART for the controller is always enabled. The UART for the SFP/SFP+ Module can be disabled when the controller needs to have access to the SFP/SFP+ Module. In addition, there is a tristate driver between the UART and the SFP/SFP+ Module, which operates as an open-drain output. The controller is also programmed to be open drain, thus preventing collisions and possible damage to the output drivers.

1.7 INA219 I²C Power Monitor

The INA219 power monitor is connected to the power rail of the SFP/SFP+ Module and measures the voltage on the SFP/SFP+ Module, as well as the current drawn and power consumption. The power monitor is connected to the I²C bus, allowing the processor to read and transfer the acquired data to the PC. The I²C address of the power monitor is set to 40_H. The I²C bus can be disconnected via jumpers (refer to **Chapter 4.1.3**).

In parallel, the I²C bus is also connected to the SFP/SFP+ Module. A separate address range is used for the internal registers on the SFP/SFP+ Module. A jumper in parallel to the shunt resistor allows the measurement resistor to be shorted.

When a PC with correct FTDI drivers is attached to the USB interface, two COM interfaces will appear. Normally the first one is the UART of the SFP/SFP+ Module, while the second one is the UART of the Atmel* ATMega328 processor.

1.8 Power Supply

The SFP Base Board is powered by a +12 V / 1 A AC/DC power supply and is protected from incorrect currents or voltages by an inrush current controller placed directly on the board.

A DC/DC converter on the SFP Base Board generates the +3.3 V system voltage. Additional DC/DC converter generates the power rails for the Aquantia* PHY AQR107 for +0.85 V, 1.2 V and 2.1 V.

2 Interfaces and Pinout

This chapter describes the connectors, headers and jumpers provided on the SFP Base Board.

2.1 SFP Module Connector J1

Connector J1 connects the SFP/SFP+ Module to the SFP Base Board.

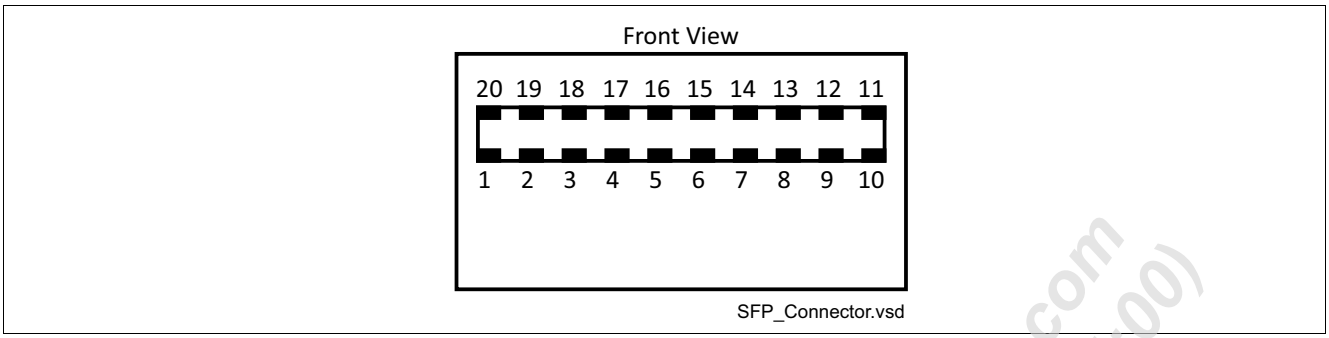

Figure 3 SFP Module Connector (J1) - Front View

Table 1 SFP Module Connector (J1)

Pin	Use	Function	Default Use	Connected to Atmel* Controller	Connected to Special Function
1	I/O	VeeT	GND	-	BOOT4 (as set by jumper J6), ASC_TX1 (when jumper J21 is in position 1-2)
2	I	TxFAULT	TxFAULT	Port PD6	ASC_TX1 (when jumper J21 is in position 5-6)
3	O	TxDisable	TxDisable	Port PD7	ASC_RX1 (when jumper J22 is in position 2-3)
4	I/O	MOD_DEF2	I2C_SDA	I2C_SDA (port PC4)	-
5	O	MOD_DEF1	I2C_SCL	I2C_SCL (port PC5)	-
6	I/O	MOD_DEF0	Module present	Port PC3	ASC_TX1 (when jumper J21 is in position 3-4)
7	O	Rate Select	“Dying Gasp” (default)	R_SEL_RST when R114 is mounted (port PC2)	ASC_RX1 (when jumper J22 is in position 1-2)
8	I	LOS	LOS	Port PB2	-
9	I	VeeR	GND	-	NTR
10	I	VeeR	GND	-	BOOT0 (as set by jumper J7)
11	I	VeeR	GND	-	-
12	O	RD-	TX_N	-	-
13	O	RD+	TX_P	-	-
14	O	VeeR	GND	-	-
15	O	VccR	+3.3 V	-	-
16	I/O	VccT	+3.3 V	-	-
17	I/O	VeeT	GND	-	-
18	I	TD+	RX_P	-	-

Table 1 SFP Module Connector (J1) (cont'd)

Pin	Use	Function	Default Use	Connected to Atmel* Controller	Connected to Special Function
19	I	TD-	RX_N	-	-
20		VeeT	GND	-	-

2.2 Power Supply Connector (J11)

The SFP Base Board has one power plug (J11), which is used to supply the complete board. The required voltage levels are derived from this source via DC/DC converters on the SFP Base Board.

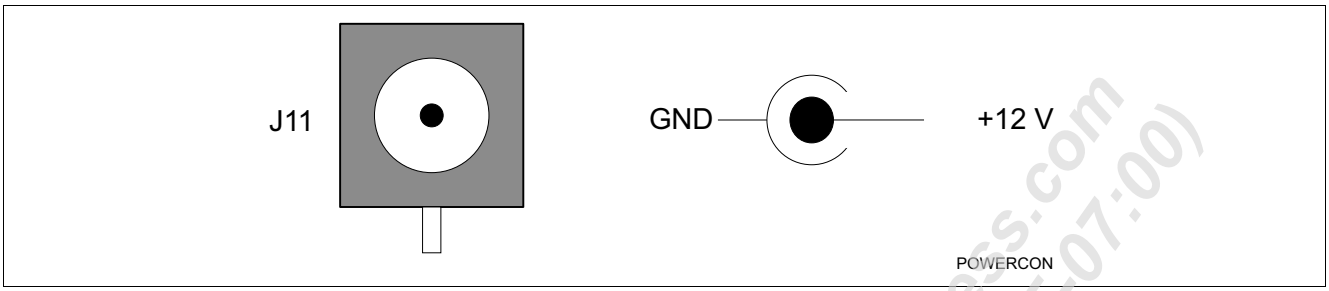

Figure 4 Power Plug (J11)

2.3 RJ-45 Ethernet Connector (J20)

A PC can be connected to the SFP Base Board via the Gigabit Ethernet jack J20. The Aquantia* PHY AQR107 operates with different speeds up to 10G.

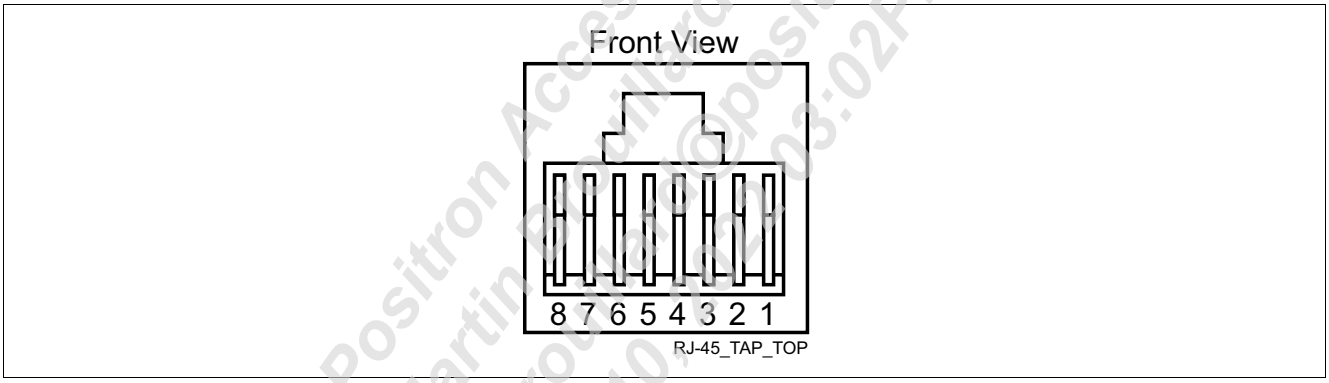

Figure 5 RJ-45 Jack (J20)

Table 2 RJ-45 Jack J20

Pin	Use	Signal
1	I/O	MX_A+
2	I/O	MX_A-
3	I/O	MX_B+
4	I/O	MX_C+
5	I/O	MX_C-
6	I/O	MX_B-
7	I/O	MX_D+
8	I/O	MX_D-

2.4 USB Interface Connector (J5)

There are two UART interfaces for control and debug information. These are connected to the Atmel* processor and to the SFP Module connector (J1) via the jumpers J19 and J21 in default mode.

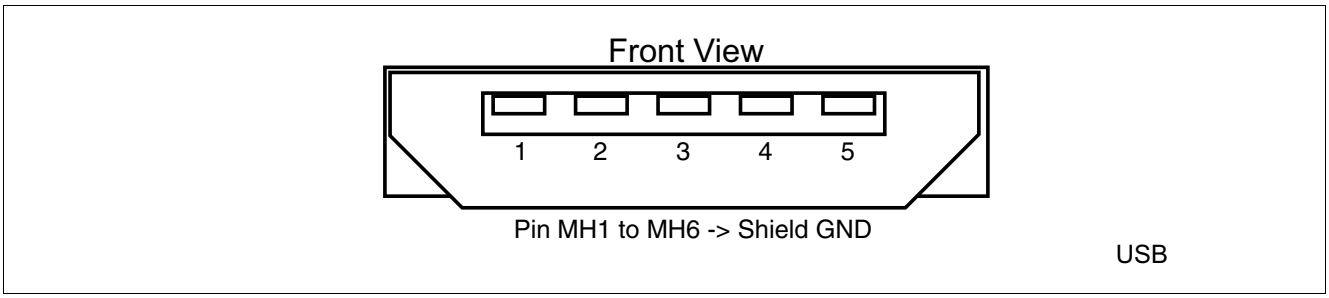

Figure 6 USB Interface Connector (J5)

Table 3 USB Interface Connector J5

Pin	Use	Function
1	I/O	VBUS +5.0 V only FTDI is self-powered
2	I/O	D-
3	I/O	D+
4	-	ID
5	I/O	GND
MH1		EARTH GND
MH2		EARTH GND
MH3	I/O	EARTH GND
MH4	I/O	EARTH GND
MH5	I/O	EARTH GND
MH6	I/O	EARTH GND

2.5 Fan Connector (J3)

There is a connector that allows a fan to be attached to the SFP Base Board. This option allows the SFP/SFP+ Module to be cooled down when it has no housing.

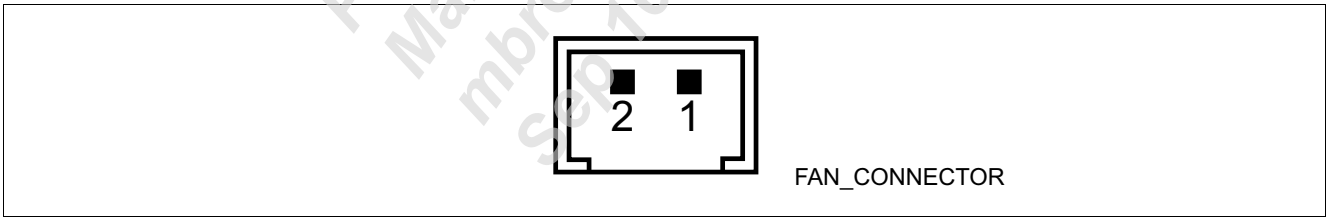

Figure 7 Fan Connector (J3)

Table 4 Fan Connector J3

Pin	Use
1	+12 V (R13_SVP reduces the power at the fan)
2	GND

2.6 I²C Bus Header (J17)

The I²C bus can be monitored via header J17.

Figure 8 I²C Bus Headers (J17)

Table 5 I²C Bus Header (J17)

Pin	Use	Function
1	I/O	+3.3 V
2	I/O	GND
3	I/O	SCL
4	I/O	SDA

2.7 Atmel* Programming Header (J18)

The programming interface can be connected to the board via J18, and is used for programming and obtaining debug information.

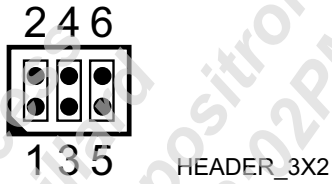

Figure 9 Atmel* Programming Header (J18)

Table 6 Atmel* Programming Header J18

Pin	Use	Function
1	O	MISO
2	I/O	+3.3 V
3	I	SCK
4	I	MOSI
5	I	RESET_N
6	I/O	GND

2.8 Analog Test Signal Header (J4)

The unused signal pins of the Atmel* analog part are connected to J4.

Figure 10 Analog Test Signal Header (J4)

Table 7 Analog Test Signal Header J4

Pin	Use	Function
1	I/O	+3.3 V
2	I/O	ADC6
3	I/O	ADC7
4	I/O	GND

2.9 RS-232 Interface Test Header (J15)

The serial asynchronous interface module for control and debug information can be connected to X3_MC. An RS-232 transceiver is connected in parallel on the SFP Base Board. By default no test pins are connected.

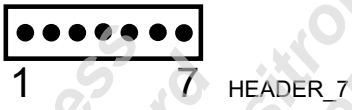

Figure 11 RS-232 Interface Test Header (J15)

Table 8 RS-232 Interface Test Header J15

Pin	Use	Function
1	I/O	+3.3 V
2	I/O	UART0_RX
3	I/O	UART0_TX
4	I/O	GND
5	I/O	UART1_TX
6	I/O	UART1_RX
7	I/O	+3.3V

2.10 SFP Signal Test Header (P1)

The control signals of the SFP/SFP+ Module are connected to P1.

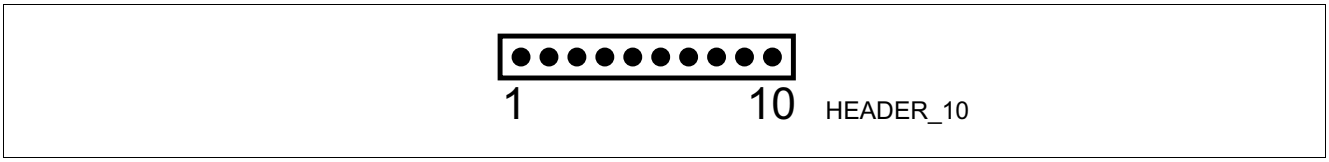

Figure 12 SFP Signal Test Header (P1)

Table 9 SFP Signal Test Header P1

Pin	Use	Function	SFP Cage Pin
1	I/O	TxFault	2
2	I/O	TxDisable	3
3	I/O	MOD_DEF2	4
4	I/O	MOD_DEF1	5
5	I/O	MOD_DEF0	6
6	I/O	UART_RX	7
7	I/O	LOSS_SD	8
8	I/O	NTR	9
9	I/O	BOOT4	10
10	I/O	GND	11

2.11 Aquantia* PHY Test Headers

2.11.1 Flash Signal Test Header (J23)

The signals between the flash memory and Aquantia* PHY AQR107 can be measured at J23.

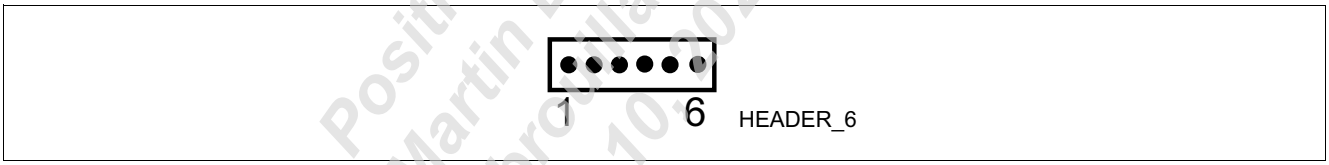

Figure 13 Flash Signal Test Header (J23)

Table 10 Flash Signal Test Header (J23)

Pin	Use	Function
1	I/O	+3.3 V
2	I/O	MOSI
3	I/O	MISO
4	I/O	SCLK
5	I/O	CS_N
6	I/O	GND

2.11.2 MDC/MDIO Test Header (J12)

The programming interface with MDC and MDIO can be measured at J12.

Figure 14 MDC/MDIO Test Header (J12)

Table 11 MDC/MDIO Test Header (J12)

Pin	Use	Function
1	I/O	MDC
2	I/O	MDIO
3	I/O	GND

2.11.3 SM Bus Test Header (J32)

The SM Bus of the Aquantia* PHY AQR107 can be accessed via J32 to download the firmware into the flash memory or measure the signals.

Figure 15 SM Bus Test Header (J32)

Table 12 SM Bus Test Header (J32)

Pin	Use	Function
1	I/O	SMB_CLK
2	I/O	SMB_DAT
3	I/O	GND

3 SFP Base Board Control

The operating mode of the SFP Base Board is controlled by the reset logic, jumpers and mounting options, as well as by the configuration registers inside the Aquantia* PHY AQR107 and the SFP/SFP+ Module.

The SFP/SFP+ Module can be accessed or configured via the Atmel* ATMega328 processor and I^2C bus. For test and debug purposes, some of the SFP interface pins can be used for alternative functions (for example, different boot mode of Intel SFP/SFP+ Module, access to ASC interface of SFP/SFP+ Module, etc.). Details are given in chapter **Chapter 4.1**. In order for these special functions to be used, the SFP/SFP+ Module must be prepared accordingly.

There are several LEDs available to indicate board operation:

- DS7: power-on LED
- DS2: reset LED
- DS3, DS4: TX, RX UART for SFP
- DS5, DS6: TX, RX UART for ATMega328 processor
- DS8 and DS9: LEDs for ATMega328 processor
- DS1 and two LEDs inside RJ-45 plug: LEDs for Aquantia* PHY

3.1 Aquantia* PHY AQR107 Control

The Aquantia* PHY AQR107 is set up using the firmware from the connected flash device.

The firmware can be downloaded via the SM bus or the MDC/MDIO interface and a special tool from Aquantia* is available for this. J24 and J25 must be opened for downloading.

The mode can also be changed by configuring the internal registers of the AQR107. These registers are accessed via the MDIO/MDC interface, which is connected to the GPIOs of the Atmel* processor as follows:

- Port PC0 (MDC)
- Port PC1 (MDIO) - push-pull or open-drain mode

A 10 kΩ pull-up resistor is connected to the MDIO line. The SFP Base Board power-on reset is connected directly to the reset input RST_N of the device.

3.2 SFP/SFP+ Module Control

The internal registers of the SFP/SFP+ Module are accessed via the I^2C bus, which is connected to the following pins:

- MOD_DEF2 (signal SDA)
- MOD_DEF1 (signal SCL)

Resistors and jumpers are used to modify the pinout and function of the SFP/SFP+ Module pins as described in **Chapter 4.1.1**. The board power-on reset is not connected directly to the reset input RST of the SFP/SFP+ Module. The Atmel* processor controls the Rate Select pin, which is used by the “dying gasp” function in normal mode.

3.3 Atmel* USB/UART Interface

The Atmel* ATMega328 processor communicates with a connected PC via the following interface:

- USB Version 2.0

Using the UART via the USB version 2.0 interface, a PC with correct FTDI drivers and a terminal program can be used to communicate with the ATMega328 processor, which interfaces with other elements as described in **Chapter 1.4**.

The UART interface on the PC must be set up as follows:

- 57600 baud
- 8 data bits
- No parity
- 1 stop bit
- No flow control

3.4 SFP/SFP+ Module USB/UART Interface

The standard SFP/SFP+ Module specification does not include the option of allowing access to the internal debug information on the module. However, the Intel SFP/SFP+ Module does allow internal debug information to be accessed from the PEB/PEF 98035 ET/98036 ET or PRX126, for further details please refer to **Chapter 4.3** and **Chapter 4.4**. A PC with a standard terminal program (for example, TeraTerm) can be used to communicate with and debug the PEB/PEF 98035 ET/98036 ET or PRX126 firmware respectively, or to download new firmware to the SFP/SFP+ Module. The boot modes can also be modified as described in **Chapter 4.1.2**.

The UART interface on the PC must be set up as follows:

- 115200 baud
- 8 data bits
- No parity
- 1 stop bit
- No flow control

4 SFP Base Board Configuration

This chapter describes how to configure the SFP Base Board, including the jumpers and mounting options.

4.1 Jumper Settings and Mounting Options for SFP/SFP+ Module

The pinout of the SFP/SFP+ Module connector, including the internal boot-mode settings, can be modified using jumpers and mounting options. A summary of the jumpers on the SFP Base Board can be found in Chapter 4.3.

4.1.1 Pinout and Function of the PRX126 SFP+ Module

Table 1 specifies the default pinout of the SFP Module connector for the EASY PRX126 module.

The EASY PRX126 supports internal boot mode on pins 2 and 10. They allow a boot mode to be set up whereby new firmware can be downloaded via the SGMII or UART interface. The UART interface of the module can be connected to the SFP Module to allow access to internal debug information. Pins MOD_DEF1 and MOD_DEF2 can be used for the I2C bus. All the pins, with the exception of SGMII-related pins, can be connected to different functions to test different types of SFP Module.

Table 13 SFP Module Connector (J1) Configuration

Pin	Use	Function	Default Use	Relevant Resistor/Jumper	Hints and Alternative Functions
1	I/O	VeeT	GND	J28 in position 1-3 and J6 in position 2-3	J28 in position 1-3 and J6 in position 1-2 for boot mode
2	I	TxFAULT	TxFAULT	J21 in position 5-6 and J6 in position 1-2[1)]	Atmel* port PD6
3	O	TxDisable	ASC_RX1	J19 in position 5-6	Atmel* port PD7 in parallel via R89 and R91 (Atmel* open-drain output)
4	I/O	MOD_DEF2	I2C_SDA	Jumper J9	Atmel* port PC4
5	O	MOD_DEF1	I2C_SCL	Jumper J8	Atmel* port PC5
6	I/O	MOD_DEF0	-	Jumper J21 in position 5-6	-
7	O	Rate Select	ASC_TX1	J19 in position 7-8	Atmel* port PC2
8	I	LOS	LOS	-	Atmel* port PB2
9	I	VeeR	GND	J22 in position 2-4	-
10	I	VeeR	GND	J26 in position 2-4	-
11	I	VeeR	GND	-	-
12	O	RD-	TX_N	-	-
13	O	RD+	TX_P	-	-
14	O	VeeR	GND	-	-
15	O	VccR	+3.3 V	-	-
16	I/O	VccT	+3.3 V	-	-
17	I/O	VeeT	GND	-	-
18	I	TD+	RX_P	-	-
19	I	TD-	RX_N	-	-
20		VeeT	GND	-	-

1) For all SFP modules employing the PRX126, such as the EASY PRX126

4.1.2 Boot-Mode Setup for PRX126 SFP+ Module

The SFP Base Board includes a special function to support different boot modes for debugging, and to download new firmware. The setup is different between EASY 98035/EASY 98036 modules and the EASY PRX126 module.

In the case of EASY 98035/EASY 98036 modules, the feature requires two GND pins (pin 1 and 10) to be used in an Intel specific mode and not for GND.

In the case of the PRX126 SFP+ Module, the boot mode pins BOOT2 and BOOT3 are connected to pin 2 of the SFP Module connector, and the PRX126 boot mode pin BOOT1 is connected to pin 10 of the SFP Module connector. BOOT0 is internally connected to GND. For the default mode of the EASY PRX126 (boot from internal flash memory), J21 must be in position 5-6, pin 10 must be connected to GND and the jumper closed.

4.1.3 I^2C Bus for SFP/SFP+ Module and Power Measurement Device

Pins MOD_DEF1 and MOD_DEF2 can be used for I^2C bus signals. Jumpers J8 and J9 must be closed.

- J8 connects signal SCL (I2C_CLK) to the SFP/SFP+ Module.
- J9 connects signal SDA (I2C_DATA) to the SFP/SFP+ Module.

The power measurement device is connected to the I^2C bus via jumpers J10 and J14.

- J10 connects signal SCL (I2C_CLK) to the power measurement device.
- J14 connects signal SDA (I2C_DATA) to the power measurement device.

4.1.4 Dying Gasp Function

The signal pin R_SEL_RST is used for the “dying gasp” function. A voltage divider on the +12 V power input allows any undervoltage condition to be detected. The divided voltage is connected to the Dying Gasp input pin within the SFP/SFP+ Module. The module is programmed to a reference voltage of 1.74 V. The Dying Gasp software routine is started if the divided voltage is under the reference voltage.

The voltage divider consists of R17 and R18 (must be mounted), and resistor R114 must be removed to enable the divider function. R114 is used for the reset function.

4.1.5 Time-of-Day Interface

The pin MOD_DEF0 (pin 6) on the SFP Module connector can also be used for the Time-of-Day (ToD) signal, which is connected to and read by the Atmel* processor. The ToD firmware feature must be enabled in the SFP/SFP+ Module by setting the corresponding register bit within the SFP/SFP+ Module via the I^2C bus.

Pin 8 on the SFP Module connector is an output and can also have two different functions. The normal function is LOS (Loss Of Signal). The second function is PPS (Pulse per Second). The PPS signal is connected to the Atmel* processor and is used to provide the correct timing for the ToD signal.

4.1.6 Configuration of Aquantia* PHY AQR107

In standard scenarios, the Aquantia* PHY AQR107 needs to be configured to the correct timing mode 1G, 2.5G, 5G or 10G. However, in special cases, the device can be configured via the MDC/MDIO interface using software. The programming is done via the MDC/MDIO interface using the Atmel* ATMega328 processor. The commands are delivered from the connected PC via the USB/UART. A pull-up resistor connected to the MDIO signal is mounted on the SFP Base Board by default.

4.1.7 Power Monitor

The +3.3 V power rail of the SFP/SFP+ Module can be monitored using the INA219 power monitor, which measures the voltage and calculates the current drawn by the SFP/SFP+ Module. Voltage, current and power values are read from registers. A 10 mΩ, 4-wire resistor is used as a shunt resistor in the rail. Jumper X1_IPM and two 0 Ω resistors (R1_IPM and R2_IPM) are placed in parallel so as to short the shunt resistor. By default, the parallel resistors are not mounted, and the jumper is mounted but left open. The jumper can be used to connect a multi-meter.

The power monitor can be read by the processor using the I^2C bus, which is connected in parallel to the SFP/SFP+ Module. The address range must be different so as to prevents collisions. The power monitor is set to address 40_H via A0 and A1. The address can be set in the range of 40_H to $4F_H$.

Two jumpers J10 and J14 connect the I^2C bus to the Atmel* processor. J10 is used for the clock, and J14 for the data line. The I^2C bus address can be modified using optional resistors (Rx_IPM, where x equals 8..15) as described in **Table 14**.

Table 14 I^2C Bus Address and Mounting Options for INA219

Address	Mounted Resistors	
	A1	**A0**
40_H [1)]	R15_IPM	R11_IPM
41_H	R15_IPM	R8_IPM
42_H	R15_IPM	R10_IPM
43_H	R15_IPM	R9_IPM
44_H	R12_IPM	R11_IPM
45_H	R12_IPM	R8_IPM

Table 14 I²C Bus Address and Mounting Options for INA219 (cont'd)

Address	Mounted Resistors	
	A1	**A0**
46_H	R12_IPM	R10_IPM
47_H	R12_IPM	R9_IPM
48_H	R14_IPM	R11_IPM
49_H	R14_IPM	R8_IPM
$4A_H$	R14_IPM	R10_IPM
$4B_H$	R14_IPM	R9_IPM
$4C_H$	R13_IPM	R11_IPM
$4D_H$	R13_IPM	R8_IPM
$4E_H$	R13_IPM	R10_IPM
$4F_H$	R13_IPM	R9_IPM

1) Default mode

4.2 Floor Plan of SFP Base Board

Figure 16 and **Figure 17** show top and bottom views of the SFP Base Board.

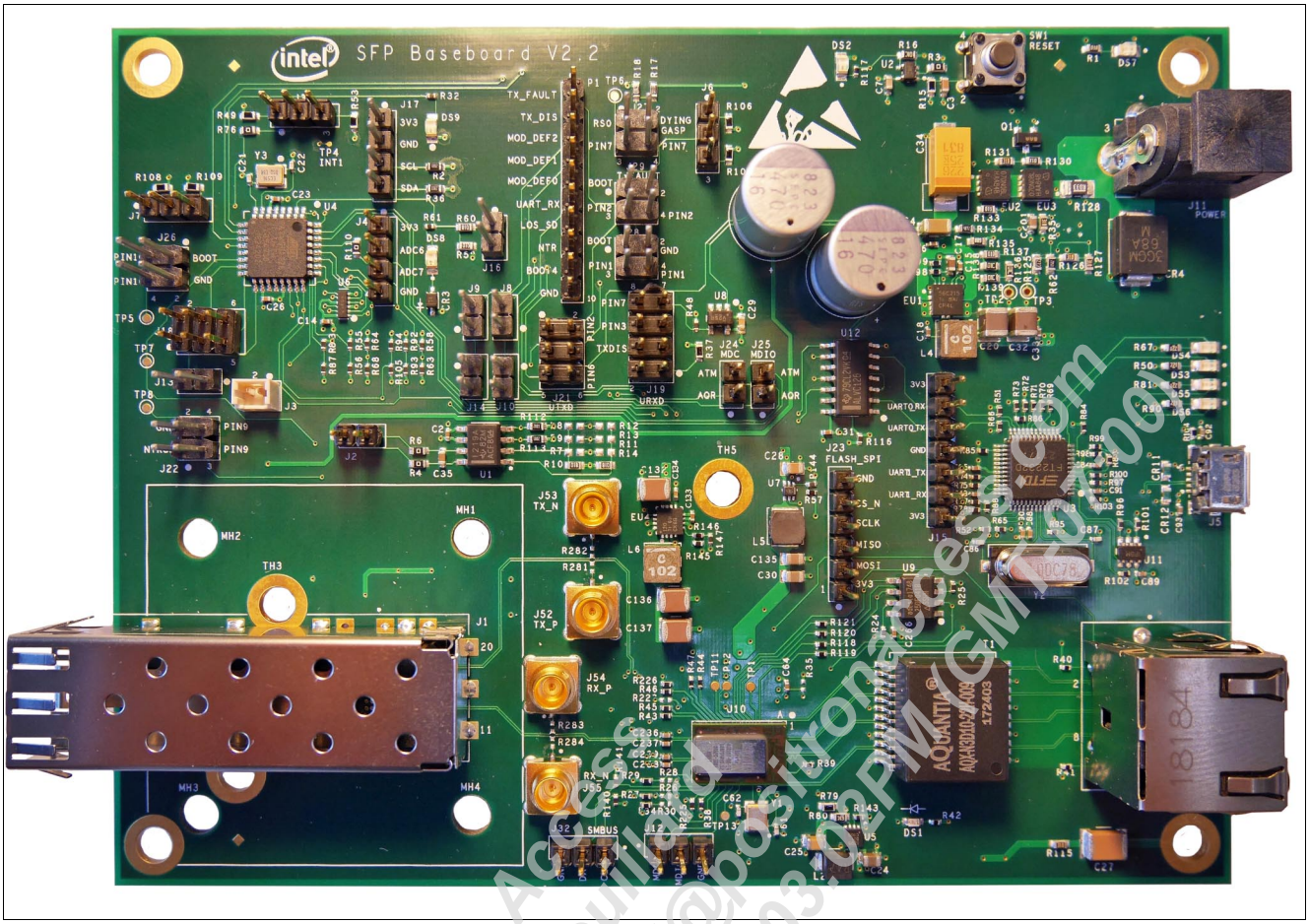

Figure 16 Top View of the SFP Base Board

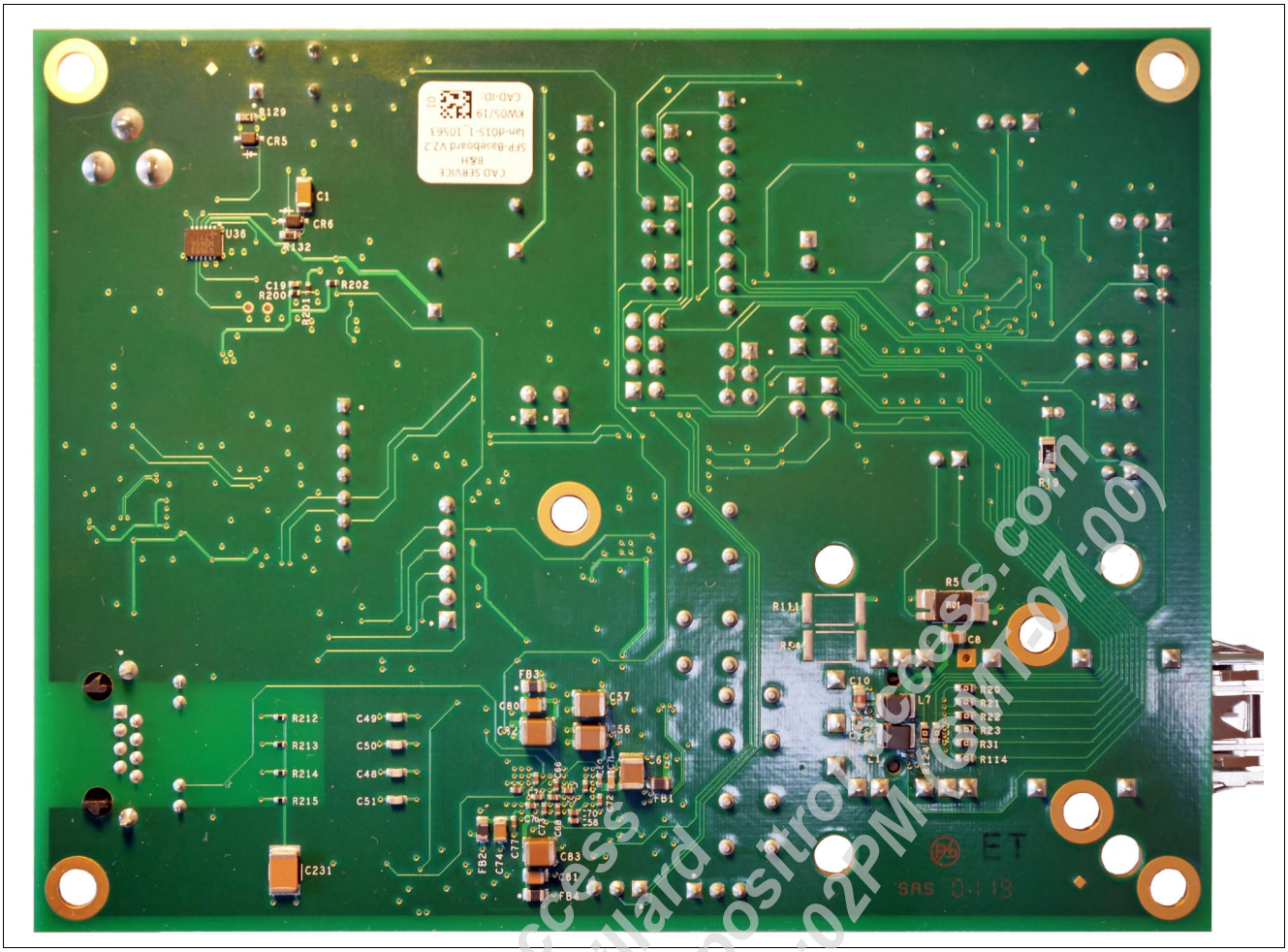

Figure 17 Bottom View of the SFP Base Board

4.3 Overview of Jumpers for 10G Applications for PRX126 SFP+ Module

Figure 18 shows the default settings of the configuration jumpers for 10G applications for the PRX126 SFP+ Module (red indicates a closed jumper) incorporating the Intel® 10G PON Chipset PRX126B0BI device. Further details are given in Table 15.

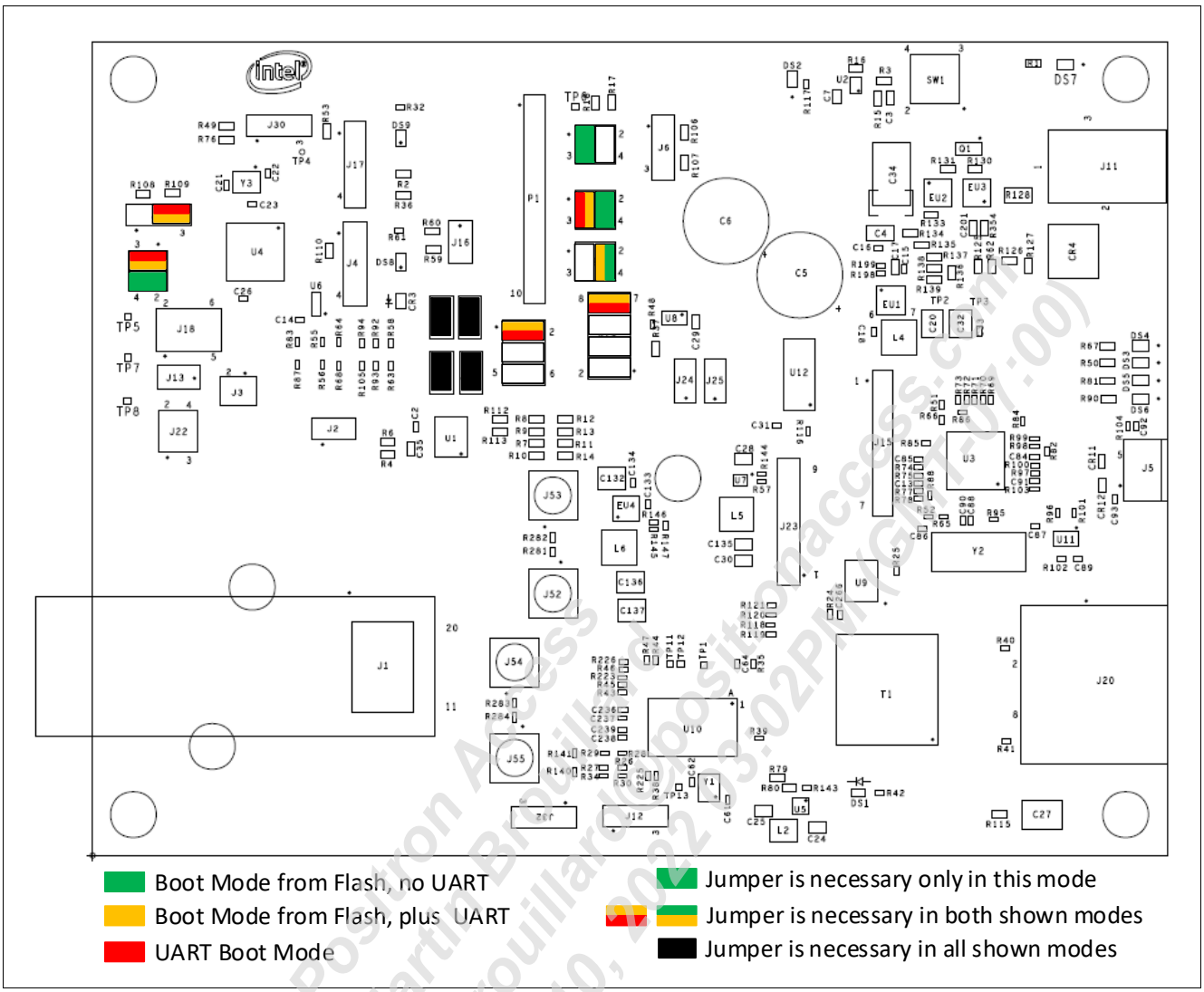

Figure 18 Configuration Jumpers for 10G Applications with PRX126B0BI (Top View of Base Board)

Table 15 Summary of Configuration Jumper Functions with PRX126B0BI for 10G Applications

Jumper	Position	Description
J8	Closed	Connects I2C_CLK to the SFP+ Module
J9	Closed	Connects I2C_DATA to the SFP+ Module
J21	Position 1-2	Connects the UART transmit signal: Pin 2 as ASC_TX1
J19	Position 7-8	Connects the UART receive signal: R_SEL_RST as ASC_RX1
J10	Optionally closed	Connects I2C_CLK to the current measurement device
J14	Optionally closed	Connects I2C_DATA to the current measurement device

Table 15 Summary of Configuration Jumper Functions with PRX126B0BI for 10G Applications (cont'd)

Jumper	Position	Description
J26	Position 2-4	Connects pin 10 of the SFP Module connector to GND (default normal connection and standard boot via internal flash memory)
	Position 1-3	Closed in UART boot mode and boot from flash memory with UART active
J28	Position 1-2	Connects pin 1 of the SFP Module connector to GND or +3.3 V (selection by J6)
J6	Position 1-2[1)] or open	Set the boot at pin 1 to high level (internal pull-up in open jumper mode)
J7	Position 2-3	Set the boot mode at pin 10 to GND

1) J6 must be set in position 1-2 when PRX126A1BI is on SFP+ Module

4.4 Overview of Jumpers for 1G Applications for EASY 98035 SFP Module

Figure 18 shows the default settings of the configuration jumpers for 1G applications for the EASY 98035 SFP Module (red indicates a closed jumper). Further details are given in Table 15.

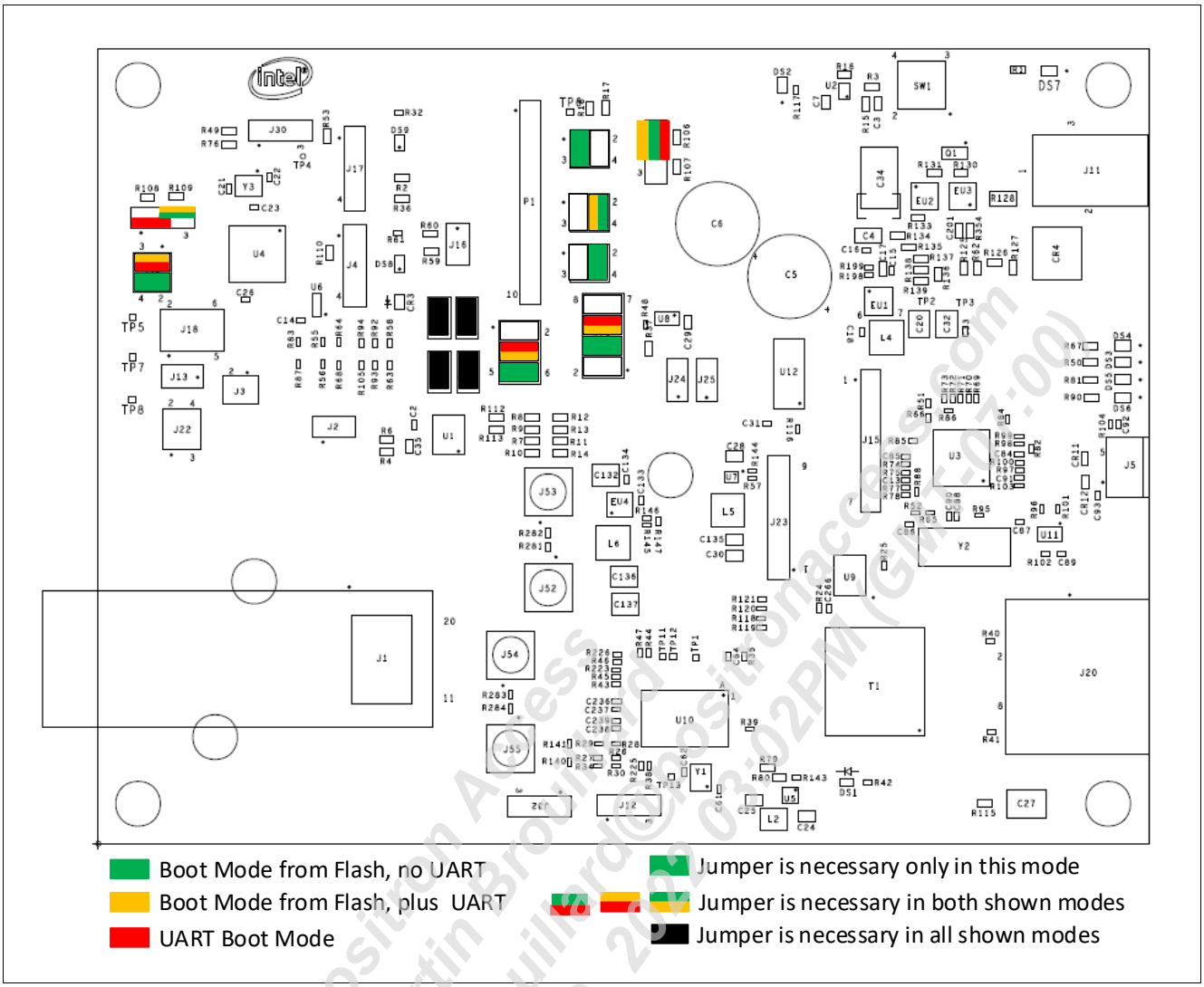

Figure 19 Configuration Jumpers for 1G Applications for EASY98035 (Top View of Base Board)

Table 16 Summary of Configuration Jumper Functions for 1G Applications for EASY98035

Jumper	Position	Description
J8	-	Connects I2C_CLK to the SFP Module
J9	-	Connects I2C_DATA to the SFP Module
J21	Position 3-4	Connects the UART transmit signal: MOD_DEF0 as ASC_TX1
	Position 5-6	Connects MOD_DEF0 to the controller (Atmel* ATMega328)
J19	Position 5-6	Connects Tx_Disable as ASC_RX
	Position 3-4	Connects Tx_Disable to the controller (Atmel* ATMega328)
J10	-	Connects I2C_CLK to the current measurement device
J14	-	Connects I2C_DATA to the current measurement device

Table 16 Summary of Configuration Jumper Functions for 1G Applications for EASY98035 (cont'd)

Jumper	Position	Description
J26	Position 2-4	Connects pin 10 of the SFP Module connector to GND (default normal connection and standard boot via internal flash memory)
	Position 1-3	Activate UART and boot mode from flash memory (see J7)
J7	Position 1-2	Used in boot mode, boot from UART
	Position 2-3	Connects pull-down to pin 10 to enable boot mode from flash memory
J28	Position 2-4	Connects pin 1 of the SFP Module connector to GND (default normal connection and standard boot via internal flash memory)
	Position 1-3	Connects pin 1 of the SFP Module connector to the level setup by J6
J6	Position 1-2	Connects pull-up to pin 1, used in all three boot modes
	Position 2-3	A pull-down resistor is not used

4.5 Overview of Jumpers for 1G Applications for EASY 98035-1588 SFP Module

Figure 18 shows the default settings of the configuration jumpers for 1G applications for EASY 98035 SFP Module (red indicates a closed jumper). Further details are given in Table 15.

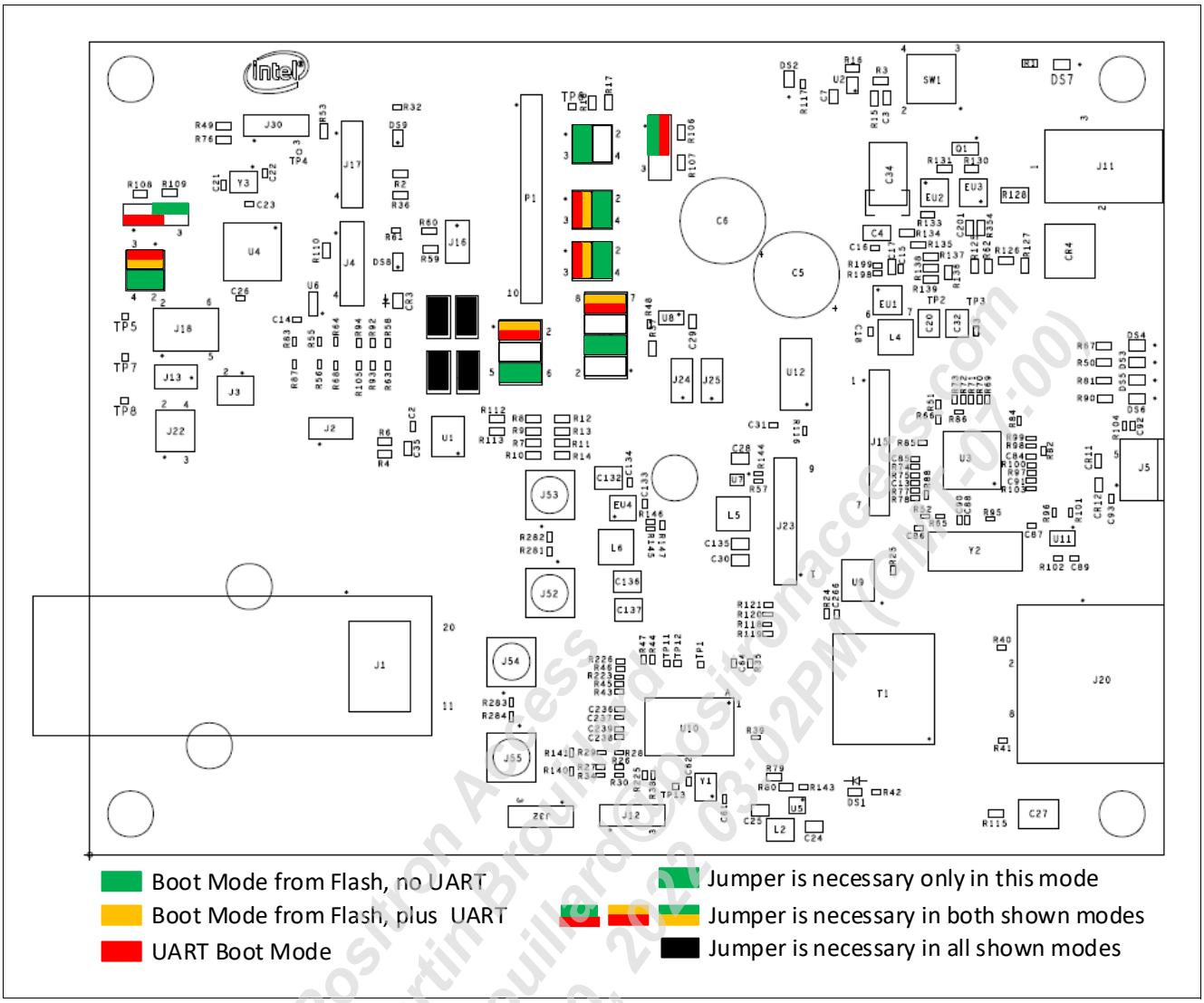

Figure 20 Configuration Jumpers for 1G Applications for EASY 98035-1588 (Top View of Base Board)

Table 17 Summary of Configuration Jumper Functions for 1G Applications with EASY 98035-1588

Jumper	Position	Description
J8	-	Connects I2C_CLK to the SFP Module.
J9	-	Connects I2C_DATA to the SFP Module.
J10	-	Connects I2C_CLK to the current measurement device.
J14	-	Connects I2C_DATA to the current measurement device.
J21	Position 1-2	Connects the UART transmit signal: TxFAULT as ASC_TX.
	Position 5-6	Connects MOD_DEF0 pin 6 to the controller (Atmel* ATMega328)
J19	Position 7-8	Connects RATE_SEL as ASC_RX
	Position 3-4	Connects Tx_disable pin 3 to the controller (Atmel* ATMega328)

Table 17 Summary of Configuration Jumper Functions for 1G Applications with EASY 98035-1588

Jumper	Position	Description
J28	Position 2-4	Connects pin 1 to GND (default)
	Position 1-3	Connects pin 1 to pull-up or -down (see jumper J6)
J29	Position 2-4	TxFault is connected to the controller (Atmel* ATMega328)
	Position 1-3	Connects pin 2 to pull-up or -down (see jumper J6
J26	Position 2-4	Connects pin 10 to GND (default mode)
	Position 1-3	Connects pin 10 to pull-up or -down (see jumper J7)
J27	Position 1-3	Connects pin 7 to Rate_SEL in the default mode.
	Position 2-4	Not used
J6	Position 1-2	Pull-up is connected to the signal to enable all three boot modes
	Position 2-3	Pull-down is connected to the signal to set up the boot mode
J7	Position 1-2	Pull-up is connected to the signal to enable boot mode from UART and flash memory
	Position 2-3	Pull-down is connected to the signal to enable boot mode from flash memory

Literature References

[1] PEB/PEF 98035 ET Version 1.3 User's Manual Hardware Description Rev. 1.6, 2016-04-08

[2] EASY 98035 SFP Reference Stick V1.2/V1.3 User's Manual Hardware Description Rev.1.0, 2013-09-12

[3] Intel® 10G PON Development Kit EASY PRX126 REF BOARD V1.2 (SFP+) Hardware Description Rev. 1.0, 2019-03-12

[4] Intel® PON Chipset Version 1.3 User's Manual Programmer's Reference Rev. 1.8, 2017-05-15

Attention: Please refer to the latest revision of the documents.

Terminology

I	
I^2C	Inter-Integrated Circuit
L	
LDO	Low Dropout
LOS	Loss of Signal
M	
MAC	Medium Access Control
MDC	Management Data Clock
MDIO	Management Data Input/Output
MSA	Multi Source Agreement Group
O	
ONT	Optical Network Termination
P	
PCB	Printed Circuit Board
PPS	Pulses per Second
S	
SFP	Small Form-Factor Pluggable
SGMII	Serial Gigabit Media-Independent Interface
T	
ToD	Time-of-Day
U	
USB	Universal Serial Bus