10G PON Chipset

10G PON Chipset PRX126 (PRX126B0BI)
10G PON Chipset PRX126 (PRX126B1BI)
10G PON Chipset PRX126 (PRX126B2BI)
10G PON Chipset PRX126 (PRX126B3BI-AV-T)

Data Sheet

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Revision History

Current:	**Revision 3.6, 2023-02-13**
Previous:	**Revision 3.5, 2022-09-08**
Page	**Major changes since Revision 3.5**
All	Added PRX126B3BI to the scope of the document.
12	Updated **Chapter 1.3 Differences between Silicon Steps**.
88	Updated **Chapter 20 Chip ID**.
119	Updated **Chapter 24.1 Chip Identification and Ordering Information**. Removed ordering codes for the B0 and B1 devices.
124	Updated **Literature References**.

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1 Overview

10G PON Chipset PRX126 is a highly integrated, cost optimized and low power consumption GPON/XGS-PON/NG-PON2/EPON/10G-EPON SFP+/SFP ONU system solution. On the line side, the device connects to an optical transceiver or an Ethernet transceiver on board via a SerDes interface. On the system side, it provides one high speed SerDes interface. Both SerDes interfaces support XFI/SFI/10G-KR/2500BASE-X/1000BASE-X/single-port USXGMII/SGMII modes. The device features real wire-speed packet switching capabilities with carrier grade QoS management independent of the packet size and the application processing performed by the on-chip CPU.

1.1 Block Diagram

Figure 1 shows the PRX126 block diagram.

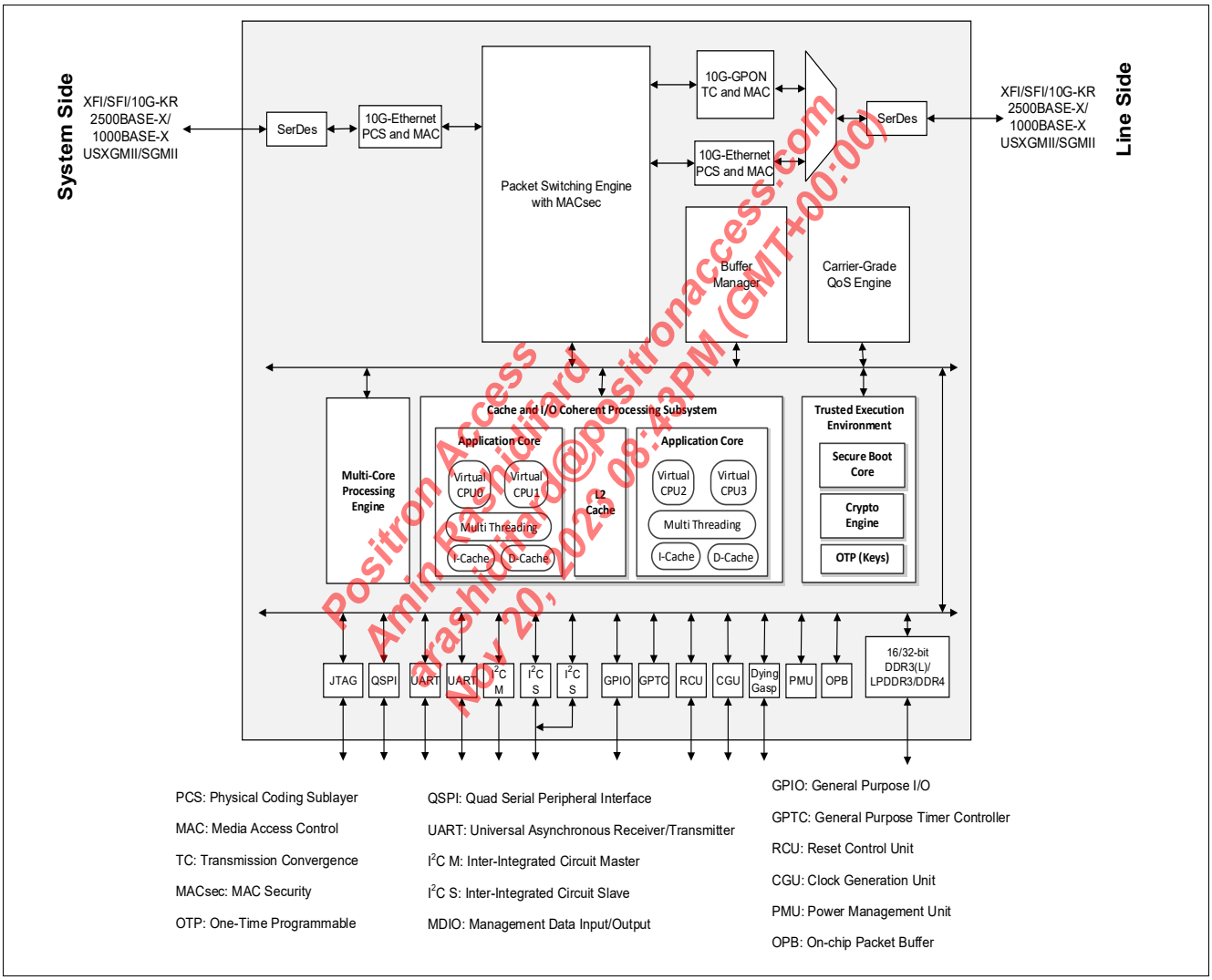


Figure 1 PRX126 Block Diagram

1.2 Features

PRX126 supports these features:

- Line side interface with one of these modes:
  - Passive Optical Network (PON) Mode: integrated transmission convergence, physical coding sublayer, MAC and SerDes connecting to an external optical transceiver; Support of GPON/XGS-PON/NG-PON2/EPON/10G-EPON SFP+/SFP standards, 256 GEM/XGEM ports, 64 T-CONTs or 16 LLIDs
  - Active Optical Network (AON) Mode: integrated Ethernet physical coding sublayer, MAC and SerDes connecting to an external optical transceiver supporting 10GBASE-R and 1000BASE-X
  - Copper wire mode: integrated Ethernet physical coding sublayer, MAC and SerDes connecting to an external Ethernet transceiver supporting 10GBASE-T or lower speed grades
  - The optical transceiver or the Ethernet transceiver is a device on board and is connected to the PRX126 device via a SerDes interface supporting XFI/SFI, 10G-KR, 2500BASE-X, 1000BASE-X, single-port USXGMII, or SGMII modes
- System side
  - One SerDes interface supporting XFI/SFI, 10G-KR, 2500BASE-X, 1000BASE-X, single-port USXGMII, or SGMII modes
- Packet switching engine
  - Bidirectional 10 Gbit/s wire-speed bridging, VLAN classification and modification, filtering and flow based classification for all valid packet sizes
  - Bidirectional 10 Gbit/s in-line MACsec encryption and decryption on one of the Ethernet interfaces
- Carrier grade QoS engine
  - Bidirectional 10 Gbit/s wire-speed for all valid packet sizes
  - RED/WRED drop polices, hierarchical shaping and scheduling
- Cache and I/O coherent processor subsystem
  - Four dual core virtual CPUs running at up to 800 MHz
  - 32 KB L1 instruction cache and 32 KB L1 data cache per core
  - 256 KB L2 cache with I/O coherency
- Trusted execution environment
  - One dedicated Secure Boot core
  - On-chip OTP module to store the root of trust assets
  - Integrated crypto engine to support encryption, decryption and true random number generation
  - Access protection
- Multiple-core processing engine
  - Integrated hardware offloading logics to enable flexible and high speed packet processing
- High speed 16 or 32-bit DDR3, DDR3L, LPDDR3, and DDR4 interface up to 2133 MT/s
- Built-in thermal management with integrated temperature sensors and overheat detection
- Integrated power-on reset detection and dying gasp detection logics
- Advanced power management capabilities
- Advanced loopback and diagnostic capabilities
- G.8275/Y.1369/IEEE 1588v2 precise time protocol support and synchronous Ethernet support
- Accurate IEEE 802.1ag and ITU-T Y.1731 Ethernet OAM delay and loss measurement hardware support
- Ambient temperature -40 to 85°C

1.3 Differences between Silicon Steps

Refer to the PRX126 errata sheet [5] which covers all silicon B-steps of the device (B0, B1, B2, and B3).

1.4 Typical Application

This section shows the typical application of the PRX126 device.

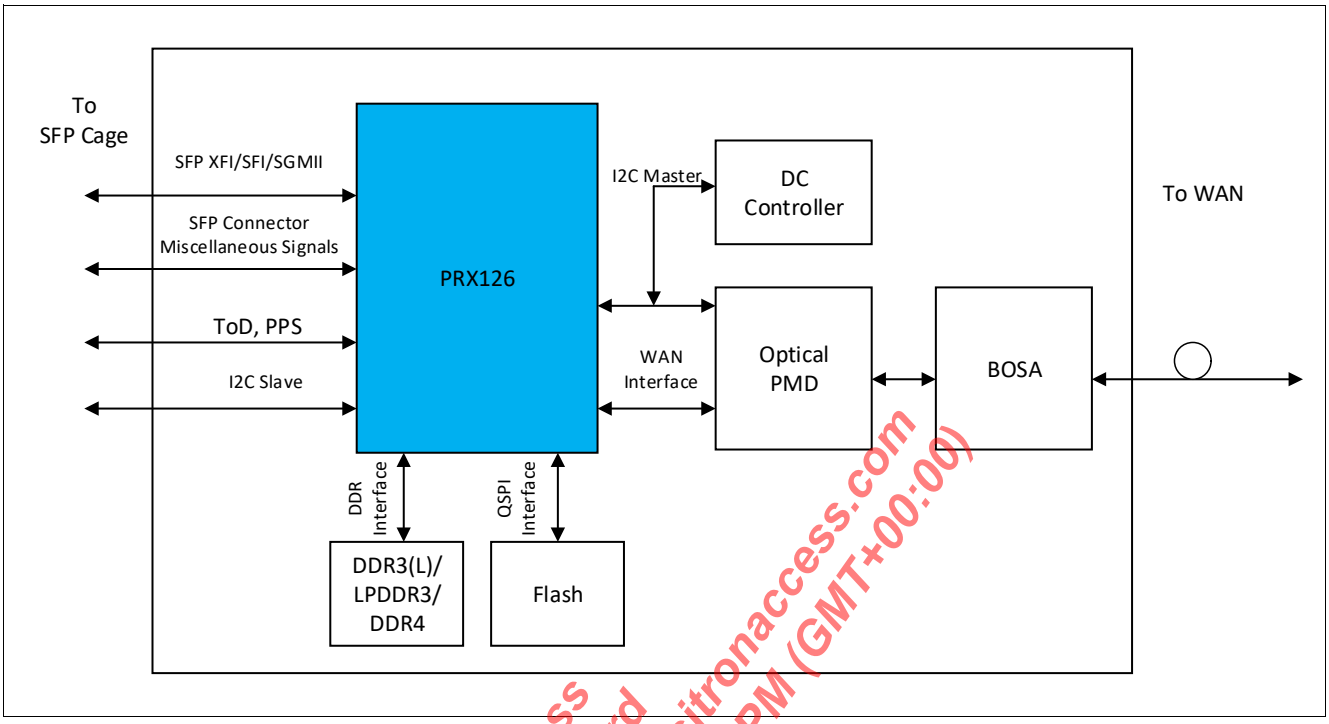


Figure 2 PRX126 Typical Application

2 Pin Descriptions

This chapter describes the pin diagram and the pin assignments in PRX126.

2.1 List of Interfaces

Table 1 summarizes the supported interfaces.

Table 1 External Signals

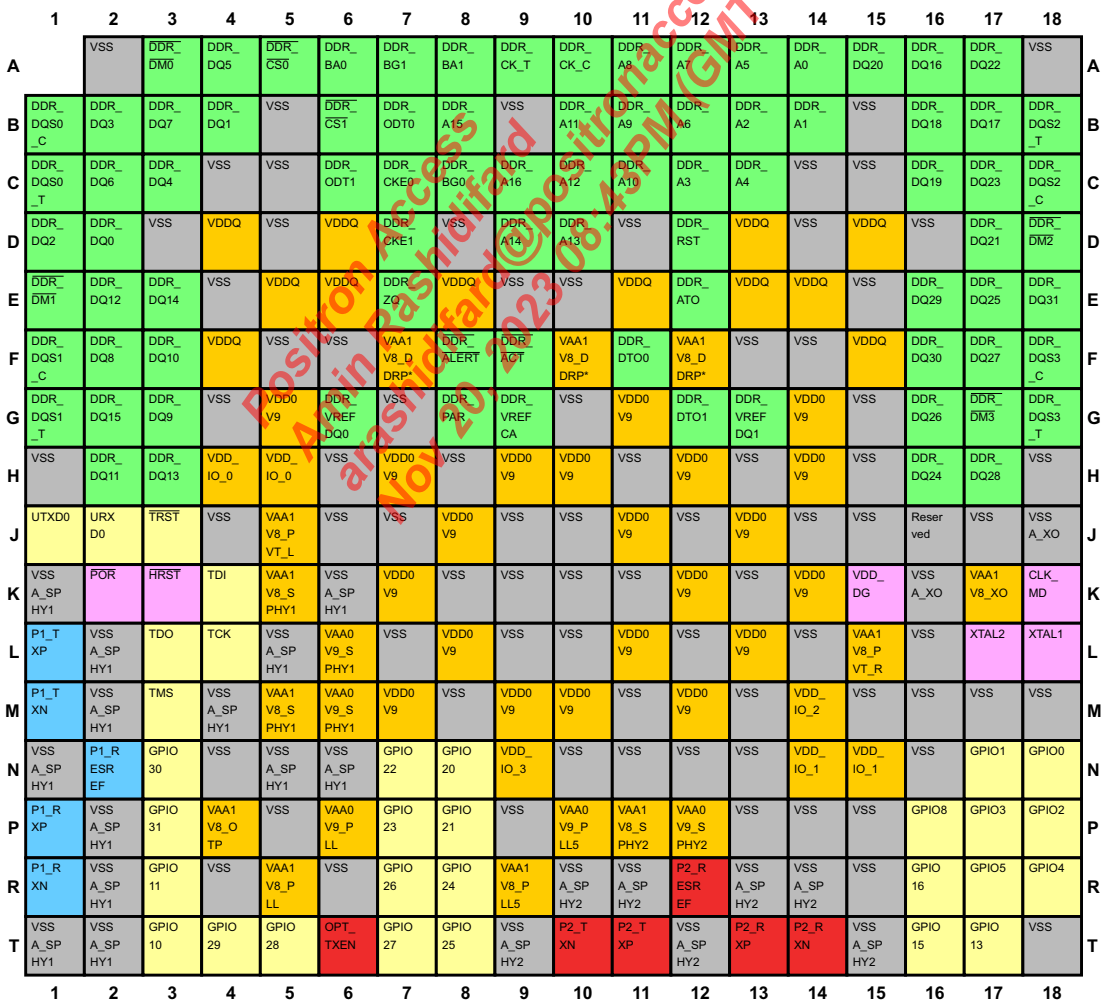
Interface	Link
WAN Signals	Table 5
SFP XFI/SFI/SGMII Signals	Table 6
SFP Connector Miscellaneous Signals	Table 7
UART Signals	Table 8
QSPI Signals	Table 9
I^2C Signals	Table 10
Clock Signals	Table 11
GPIO Signals	Table 12
JTAG Signals	Table 13
16/32-bit DDR SDRAM Signals	Table 14
Reset Signals	Table 15
Power Supply	Table 16
Ground	Table 17
Dying Gasp	Table 18
Reserved Signals	Table 19

2.2 Ball Diagram

Figure 3 shows the ball diagram. **Table 2** lists the ball diagram color codes.

Table 2 Ball Diagram Color Codes

Color	Description
White in outer ring	Unpopulated Balls
Green	DDR Interface
Orange	Power
Red	WAN Signals
Blue	SFP Connector XFI/SFI/SGMII Signals
Pink	Clock, Reset, Dying Gasp
Yellow	GPIO, JTAG Interface
Grey	Ground, Fuse, Reserved



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		VSS	DDR_ DM0	DDR_ DQ5	DDR_ CS0	DDR_ BA0	DDR_ BG1	DDR_ BA1	DDR_ CK_T	DDR_ CK_C	DDR_ A8	DDR_ A7	DDR_ A5	DDR_ A0	DDR_ DQ20	DDR_ DQ16	DDR_ DQ22	VSS	A
B	DDR_ DQS0 _C	DDR_ DQ3	DDR_ DQ7	DDR_ DQ1	VSS	DDR_ CST	DDR_ ODT0	DDR_ A15	VSS	DDR_ A11	DDR_ A9	DDR_ A6	DDR_ A2	DDR_ A1	VSS	DDR_ DQ18	DDR_ DQ17	DDR_ DQS2 _T	B
C	DDR_ DQS0 _T	DDR_ DQ6	DDR_ DQ4	VSS	VSS	DDR_ ODT1	DDR_ CKE0	DDR_ BG0	DDR_ A16	DDR_ A12	DDR_ A10	DDR_ A3	DDR_ A4	VSS	VSS	DDR_ DQ19	DDR_ DQ23	DDR_ DQS2 _C	C
D	DDR_ DQ2	DDR_ DQ0	VSS	VDDQ	VSS	VDDQ	DDR_ CKE1	VSS	DDR_ A14	DDR_ A13	VSS	DDR_ RST	VDDQ	VSS	VDDQ	VSS	DDR_ DQ21	DDR_ DM2	D
E	DDR_ DM1	DDR_ DQ12	DDR_ DQ14	VSS	VDDQ	VDDQ	DDR_ ZQ	VDDQ	VSS	VSS	VDDQ	DDR_ ATO	VDDQ	VDDQ	VSS	DDR_ DQ29	DDR_ DQ25	DDR_ DQ31	E
F	DDR_ DQS1 _C	DDR_ DQ8	DDR_ DQ10	VDDQ	VSS	VSS	VAA1 V8_D DRP*	DDR_ ALERT	DDR_ ACT	VAA1 V8_D DRP*	DDR_ DTO0	VAA1 V8_D DRP*	VSS	VSS	VDDQ	DDR_ DQ30	DDR_ DQ27	DDR_ DQS3 _C	F
G	DDR_ DQS1 _T	DDR_ DQ15	DDR_ DQ9	VSS	VDD0 V9	DDR_ VREF DQ0	VSS	DDR_ PAR	DDR_ VREF CA	VSS	VDD0 V9	DDR_ DTO1	DDR_ VREF DQ1	VDD0 V9	VSS	DDR_ DQ26	DDR_ DM3	DDR_ DQS3 _T	G
H	VSS	DDR_ DQ11	DDR_ DQ13	VDD_ IO_0	VDD_ IO_0	VSS	VDD0 V9	VSS	VDD0 V9	VDD0 V9	VSS	VDD0 V9	VSS	VDD0 V9	VSS	DDR_ DQ24	DDR_ DQ28	VSS	H
J	UTXD0	URX D0	TRST	VSS	VAA1 V8_P VT_L	VSS	VSS	VDD0 V9	VSS	VSS	VDD0 V9	VSS	VDD0 V9	VSS	VSS	Reser ved	VSS	VSS A_XO	J
K	VSS A_SP HY1	POR	HRST	TDI	VAA1 V8_S PHY1	VSS A_SP HY1	VDD0 V9	VSS	VSS	VSS	VSS	VDD0 V9	VSS	VDD0 V9	VDD_ DG	VSS A_XO	VAA1 V8_XO	CLK_ MD	K
L	P1_T XP	VSS A_SP HY1	TDO	TCK	VSS A_SP HY1	VAA0 V9_S PHY1	VSS	VDD0 V9	VSS	VSS	VDD0 V9	VSS	VDD0 V9	VSS	VAA1 V8_P VT_R	VSS	XTAL2	XTAL1	L
M	P1_T XN	VSS A_SP HY1	TMS	VSS A_SP HY1	VAA1 V8_S PHY1	VAA0 V9_S PHY1	VDD0 V9	VSS	VDD0 V9	VDD0 V9	VSS	VDD0 V9	VSS	VDD_ IO_2	VSS	VSS	VSS	VSS	M
N	VSS A_SP HY1	P1_R ESR EF	GPIO 30	VSS	VSS A_SP HY1	VSS A_SP HY1	GPIO 22	GPIO 20	VDD_ IO_3	VSS	VSS	VSS	VSS	VDD_ IO_1	VDD_ IO_1	VSS	GPIO1	GPIO0	N
P	P1_R XP	VSS A_SP HY1	GPIO 31	VAA1 V8_O TP	VSS	VAA0 V9_P LL	GPIO 23	GPIO 21	VSS	VAA0 V9_P LL5	VAA1 V8_S PHY2	VAA0 V9_S PHY2	VSS	VSS	VSS	GPIO8	GPIO3	GPIO2	P
R	P1_R XN	VSS A_SP HY1	GPIO 11	VSS	VAA1 V8_P LL	VSS	GPIO 26	GPIO 24	VAA1 V8_P LL5	VSS A_SP HY2	VSS A_SP HY2	P2_R ESR EF	VSS A_SP HY2	VSS A_SP HY2	VSS	GPIO 16	GPIO5	GPIO4	R
T	VSS A_SP HY1	VSS A_SP HY1	GPIO 10	GPIO 29	GPIO 28	OPT_ TXEN	GPIO 27	GPIO 25	VSS A_SP HY2	P2_T XN	P2_T XP	VSS A_SP HY2	P2_R XP	P2_R XN	VSS A_SP HY2	GPIO 15	GPIO 13	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 3 Ball Diagram for PG-VF2RBGA-287 (Top View)

2.3 Ball (Pin) Function Descriptions

Use these abbreviations for the I/O table.

Table 3 Pin Type Abbreviations

Abbreviations	Description	Analog/Digital Levels
I	Standard Input-only pin	Digital
O	Standard Output-only pin	Digital
I/O	Standard bidirectional Input/Output pin	Digital
AI	Input pin	Analog
AO	Output pin	Analog
AI/O	Bidirectional Input/Output pin	Analog
PWR	Power	N/A
GND	Ground	N/A
MCL	Must be connected to Low (JEDEC Standard).	N/A
MCH	Must be connected to High (JEDEC Standard).	N/A
NU	Not Usable (JEDEC Standard)	N/A
NC	Not Connected (JEDEC Standard). Do not connect in board design.	N/A
Prg	Programmable pin (Input, Output or Bidirectional)	Digital

Table 4 Buffer Type Abbreviations

Abbreviations	Description
A	Analog characteristics
Z	High impedance
Prg	Programmable The OD/PP and PU/PD options are programmable.
PU	Pull-up (internal, weak)
PD	Pull-down (internal, weak)
TS	Tristate capability The corresponding pin has three operational states: Low, high, and high-impedance.
OD	Open-Drain The corresponding pin has two operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An internal or external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull The corresponding pin has two operational states: Active-low and Active-high (identical to Output with no type attribute).

2.3.1 WAN Signals

Table 5 lists the WAN signals.

To maximize interoperability even in inadequate wiring environments, the PRX126 device supports the inversion of the logical sense of the positive and negative in the differential data pair.

Table 5 WAN Signals

Ball No.	Name	Pin Type	Buffer Type	Function
Signal Group Analog				
T11	**P2_TXP**	AO	A	**Differential Transmit Data Pair Positive**
T10	**P2_TXN**	AO	A	**Differential Transmit Data Pair Negative**
T13	**P2_RXP**	AI	A	**Differential Receive Data Pair Positive**
T14	**P2_RXN**	AI	A	**Differential Receive Data Pair Negative**
R12	**P2_RESREF**	AI/O	A	**Reference Resistor** *Note: Connect to a 200 Ω external resistor with ±1% accuracy.*
Signal Group Digital				
T6	**OPT_TXEN**	I/O	PP	**Optical PMD TX Burst Enable** Indicating WAN TX burst enable to the external optical transceiver.
N8	**OPT_RX_LOS**	I	Prg	**Optical PMD RX LOS** It is an input signal from the external optical transceiver. It shares the pin with other functionality on GPIO20.
N7	**OPT_TX_FAULT**	I	Prg	**Optical PMD TX Fault** It is an input signal from the external optical transceiver. It shares the pin with other functionality on GPIO22.
P7	**OPT_TX_SD**	I	Prg	**Optical PMD TX Signal Detected** It is an input signal from the external optical transceiver. It shares the pin with other functionality on GPIO23.
R8	**OPT_TX_PUP**	I/O	Prg	**Optical PMD TX Power Up** It is connected to the external optical transceiver. It shares the pin with other functionality on GPIO24.

2.3.2 SFP XFI/SFI/SGMII Signals

Table 6 lists the SFP XFI/SFI/SGMII signals.

To maximize interoperability even in inadequate wiring environments, the PRX126 device supports the inversion of the logical sense of the positive and negative in the differential data pair.

Table 6 SFP XFI/SFI/SGMII Signals

Ball No.	Name	Pin Type	Buffer Type	Function
Signal Group Analog				
L1	**P1_TXP**	AO	A	**Differential Transmit Data Pair Positive**
M1	**P1_TXN**	AO	A	**Differential Transmit Data Pair Negative**
P1	**P1_RXP**	AI	A	**Differential Receive Data Pair Positive**
R1	**P1_RXN**	AI	A	**Differential Receive Data Pair Negative**
N2	**P1_RESREF**	AI/O	A	**Reference Resistor** *Note: Connect to a 200 Ω external resistor with ±1% accuracy.*

2.3.3 SFP Connector Miscellaneous Signals

Table 7 SFP Connector Miscellaneous Signals

Pin No.	Name	Pin Type	Buffer Type	Function
P8	**OPT_TX_DIS_SFP**	I/O	Prg	**Optical PMD TX Disable SFP** It is connected to SFP/SFP+ module connector. It shares the pin with other functionalities on GPIO21.
T8	**OPT_RX_SD_SFP**	I/O	Prg	**Optical PMD RX Signal Detected SFP** It is connected to SFP/SFP+ module connector. It shares the pin with other functionalities on GPIO25.

2.3.4 UART Signals

There are two sets of UART external interfaces. Multiple UART modules are multiplexed to these two external UART interfaces.

Table 8 UART Signals

Pin No.	Name	Pin Type	Buffer Type	Function
J2	**URXD0**	I	–	**SoC UART #0 Receive Data** SoC UART instance #0 interface receives data
	URXD_QOS			**QoS Engine Debug UART Receive Data** QoS engine processor debug interface receives data
	URXD0_PON			**PON Subsystem UART #0 Receive Data** PON subsystem UART instance #0 processor debug interface receives data
	URXD1			**SoC UART #1 Receive Data** SoC UART instance #1 interface receives data
	URXD1_PON			**PON Subsystem UART #1 Receive Data** PON subsystem UART instance #1 interface receives data
	URXD_TEP			**Secure Boot Core Debug Receive Data** Secure Boot core UART debug interface receives data
J1	**UTXD0**	O	PU	**SoC UART #0 Transmit Data** SoC UART instance #0 interface transmits data *Note: This interface is used for pin strapping BOOT3.*
	UTXD_QOS			**QoS Engine Debug UART Transmit Data** QoS engine processor debug interface transmits data
	UTXD0_PON			**PON Subsystem UART #0 Transmit Data** PON subsystem UART instance #0 processor debug interface UART transmits data
	UTXD1			**SoC UART #1 Transmit Data** SoC UART instance #1 interface transmits data
	UTXD1_PON			**PON Subsystem UART #1 Transmit Data** PON subsystem UART instance #1 interface transmits data
	UTXD_TEP			**Secure Boot Core Debug Transmit Data** Secure Boot core UART debug transmits data

Table 8 UART Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
N3	**URXD1**	I	Prg	**SoC UART #1 Receive Data** SoC UART instance #1 interface receives data. It shares the pin with other functionalities on GPIO30.
	URXD1_PON			**PON Subsystem UART #1 Receive Data** PON subsystem UART instance #1 interface receives data. It shares the pin with other functionalities on GPIO30.
	URXD_TEP			**Secure Boot Core Debug Receive Data** Secure Boot core UART debug interface receives data. It shares the pin with other functionalities on GPIO30.
	URXD_QOS			**QoS Engine Debug UART Receive Data** QoS engine processor debug interface receives data. It shares the pin with other functionalities on GPIO30.
	URXD0_PON			**PON Subsystem UART #0 Receive Data** PON subsystem UART instance #0 processor debug interface receives data. It shares the pin with other functionalities on GPIO30.
P3	**UTXD1**	O	Prg	**SoC UART #1 Transmit Data** SoC UART instance # 1 interface transmits data. It shares the pin with other functionalities on GPIO31.
	UTXD1_PON			**PON Subsystem UART #1 Transmit Data** PON subsystem UART instance #1 interface transmits data. It shares the pin with other functionalities on GPIO31.
	UTXD_TEP			**Secure Boot Core Debug Transmit Data** Secure Boot core UART debug transmits data. It shares the pin with other functionalities on GPIO31.
	UTXD_QOS			**QoS Engine Debug UART Transmit Data** QoS engine processor debug interface transmits data. It shares the pin with other functionalities on GPIO31.
	UTXD0_PON			**PON Subsystem UART #0 Transmit Data** PON subsystem UART instance #0 processor debug interface UART transmits data. It shares the pin with other functionalities on GPIO31.

2.3.5 QSPI Signals

Table 8 lists the QSPI signals.

Table 9 QSPI Signals

Pin No.	Name	Pin Type	Buffer Type	Function
N18	**QSCK**	O	Prg	**QSPI Clock** QSPI clock output. It shares the pin with other functionalities on GPIO0.
N17	**QSCS**	O	Prg	**QSPI Chip Select** QSPI chip select signal. It shares the pin with other functionalities on GPIO1. *Note: The operational state is Active-low.*
P18	**QSIO0**	I/O	Prg	**QSPI IO Bit 0** QSPI interface serial data input or serial input/output bit 0 for dual or quad I/O mode. It shares the pin with other functionalities on GPIO2.
P17	**QSIO1**	I/O	Prg	**QSPI IO Bit 1** QSPI interface serial data output or serial input/output bit 1 for dual or quad I/O mode. It shares the pin with other functionalities on GPIO3.
R18	**QSIO2**	I/O	Prg	**QSPI IO Bit 2** QSPI interface hardware write protection or serial input/output bit 2 for quad I/O mode. It shares the pin with other functionalities on GPIO4.
R17	**QSIO3**	I/O	Prg	**QSPI IO Bit 3** QSPI interface no connection or serial input/output bit 3 for quad I/O mode. It shares the pin with other functionalities on GPIO5.

2.3.6 I²C Signals

There are two sets of I²C external interfaces.

Table 10 I²C Signals

Pin No.	Name	Pin Type	Buffer Type	Function
R7	**I2C0_SCL**	I/O	Prg	**I²C Master 0 Serial Clock Line (SCL)** I²C master instance #0 clock. It shares the pin with other functionalities on GPIO26.
T7	**I2C0_SDA**	I/O	Prg	**I²C Master 0 Serial Data (SDA)** I²C master instance #0 data. It shares the pin with other functionalities on GPIO27.
T3	**I2C1_SCL**	I/O	Prg	**I²C Slave 1 Serial Clock Line (SCL)** Both I²C slave instance #1 and slave instance I²C #2 are connected to this interface. It shares the pin with other functionalities on GPIO10.
R3	**I2C1_SDA**	I/O	Prg	**I²C Slave 1 Serial Data (SDA)** Both I²C slave instance #1 and I²C slave instance #2 are connected to this interface. It shares the pin with other functionalities on GPIO11.

2.3.7 Clock Signals

Table 11 lists the clock signals.

Table 11 Clock Signals

Ball No.	Name	Pin Type	Buffer Type	Function
L18	**XTAL1**	AI	A	**External Crystal Input or Differential Clock Positive Input**
L17	**XTAL2**	AO/AI	A	**External Crystal Output or Different Clock Negative Input**
K18	**CLK_MD**	AI	A	**Clock Mode Select** This pin selects external crystal or direct clock drive mode. This pin is in the VAA1V8_XO voltage domain. 1_D **Crystal** mode 0_D **Clock** direct clock drive mode
T5	**GPC1**	Prg	Prg	**General Purpose Clock 1** General purpose clock for synchronous Ethernet or external devices. It shares the pin with other functionalities on GPIO28.
T4	**PPS**	Prg	Prg	**Pulse Per Second** Pulse per second (1PPS). It shares the pin with other functionalities on GPIO29.

2.3.8 General Purpose I/O Signals

It is possible to use general purpose I/O pins in input mode as external interrupt inputs.

There are multiple alternative functions for each GPIO. See **GPIO Functions** for information about multiplexing.

Table 12 GPIO Signals

Pin No.	Name	Pin Type	Buffer Type	Function
N18	**GPIO0**	O	Prg	**General Purpose IO Bit 0** It is used for output pin. The output characteristic is either Open-Drain or Push-Pull. *Note: This signal is used for pin strapping BOOT0.*
N17	**GPIO1**	O	Prg	**General Purpose IO Bit 1** It is used for output pin. The output characteristic is either Open-Drain or Push-Pull. *Note: This signal is used for pin strapping BOOT0.*
P18	**GPIO2**	Prg	Prg	**General Purpose IO Bit 2** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
P17	**GPIO3**	Prg	Prg	**General Purpose IO Bit 3** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
R18	**GPIO4**	Prg	Prg	**General Purpose IO Bit 4** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
R17	**GPIO5**	Prg	Prg	**General Purpose IO Bit 5** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.

Table 12 GPIO Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
P16	**GPIO8**	Prg	Prg	**General Purpose IO Bit 8** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
T3	**GPIO10**	Prg	Prg	**General Purpose IO Bit 10** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
R3	**GPIO11**	Prg	Prg	**General Purpose IO Bit 11** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
T17	**GPIO13**	O	Prg	**General Purpose IO Bit 13** It is used for output pin. The output characteristic is either Open-Drain or Push-Pull. *Note: This signal is used for pin strapping ENDIAN_BOOT.*
T16	**GPIO15**	O	Prg	**General Purpose IO Bit 15** The output characteristic is either Open-Drain or Push-Pull. *Note: This signal is used for pin strapping 1V8_BOOT.*
R16	**GPIO16**	O	Prg	**General Purpose IO Bit 16** It is used for output pin. The output characteristic is either Open-Drain or Push-Pull. *Note: This signal is used for pin strapping BOOT1.*
N8	**GPIO20**	Prg	Prg	**General Purpose IO Bit 20** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
P8	**GPIO21**	Prg	Prg	**General Purpose IO Bit 21** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
N7	**GPIO22**	Prg	Prg	**General Purpose IO Bit 22** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
P7	**GPIO23**	Prg	Prg	**General Purpose IO Bit 23** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
R8	**GPIO24**	Prg	Prg	**General Purpose IO Bit 23** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
T8	**GPIO25**	Prg	Prg	**General Purpose IO Bit 25** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
R7	**GPIO26**	Prg	Prg	**General Purpose IO Bit 26** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
T7	**GPIO27**	Prg	Prg	**General Purpose IO Bit 27** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.

Table 12 GPIO Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
T5	**GPIO28**	Prg	Prg	**General Purpose IO Bit 28** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
T4	**GPIO29**	Prg	Prg	**General Purpose IO Bit 29** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
N3	**GPIO30**	Prg	Prg	**General Purpose IO Bit 30** It is used either in input or output mode. The output characteristic is either Open-Drain or Push-Pull.
P3	**GPIO31**	O	Prg	**General Purpose IO Bit 31** It is used for output pin. The output characteristic is either Open-Drain or Push-Pull. *Note: This signal is used for pin strapping BOOT2.*

2.3.9 JTAG Signals

Table 13 describes the JTAG interface.

Table 13 JTAG Signals

Ball No.	Name	Pin Type	Buffer Type	Function
J3	**$\overline{\text{TRST}}$**	I	PU	**JTAG Reset** **Notes** *1. The operational state is Active-low.* *2. When the JTAG interface is not in use this pin must be connected to V_{SS}.* *3. A low-to-high transition of the TRST pin latches the JTAG mode (depending on the bootstrap setting of pin **TDO**).*
K4	**TDI**	I	PU	**JTAG Test Data Input**
L3	**TDO**	O	PD	**JTAG Test Data Output** There is a boot strap setting on this pin. This pin is used to determine the interface. 0 = Reserved; 1 = JTAG Test Mode
M3	**TMS**	I	PU	**JTAG Test Mode Select**
L4	**TCK**	I	–	**JTAG Test Clock**

2.3.10 DDR-SDRAM Signals

Table 14 describes the double data rate (DDR) SDRAM interface.

Table 14 DDR-SDRAM Signals

Ball No.	Name	Pin Type	Buffer Type	Function
E18	**DDR_DQ31**	I/O	–	**DDR Data Bus [31:16]**
F16	**DDR_DQ30**	I/O	–	
E16	**DDR_DQ29**	I/O	–	
H17	**DDR_DQ28**	I/O	–	
F17	**DDR_DQ27**	I/O	–	
G16	**DDR_DQ26**	I/O	–	
E17	**DDR_DQ25**	I/O	–	
H16	**DDR_DQ24**	I/O	–	
C17	**DDR_DQ23**	I/O	–	
A17	**DDR_DQ22**	I/O	–	
D17	**DDR_DQ21**	I/O	–	
A15	**DDR_DQ20**	I/O	–	
C16	**DDR_DQ19**	I/O	–	
B16	**DDR_DQ18**	I/O	–	
B17	**DDR_DQ17**	I/O	–	
A16	**DDR_DQ16**	I/O	–	
G2	**DDR_DQ15**	I/O	–	**DDR Data Bus [15:0]**
E3	**DDR_DQ14**	I/O	–	
H3	**DDR_DQ13**	I/O	–	
E2	**DDR_DQ12**	I/O	–	
H2	**DDR_DQ11**	I/O	–	
F3	**DDR_DQ10**	I/O	–	
G3	**DDR_DQ9**	I/O	–	
F2	**DDR_DQ8**	I/O	–	
B3	**DDR_DQ7**	I/O	–	
C2	**DDR_DQ6**	I/O	–	
A4	**DDR_DQ5**	I/O	–	
C3	**DDR_DQ4**	I/O	–	
B2	**DDR_DQ3**	I/O	–	
D1	**DDR_DQ2**	I/O	–	
B4	**DDR_DQ1**	I/O	–	
D2	**DDR_DQ0**	I/O	–	
C9	**DDR_A16**	O	–	**DDR4: A16** DDR3: Row Address Strobe (RAS) *Note: The operational state is Active-low for DDR3 RAS.*

Table 14 DDR-SDRAM Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
B8	**DDR_A15**	O	–	**DDR4: A15** DDR3: Column Address Strobe (CAS) *Note: The operational state is Active-low for DDR3 CAS.*
D9	**DDR_A14**	O	–	**DDR4: A14** DDR3: Write enable (WE) *Note: The operational state is Active-low for DDR3 WE.*
D10	**DDR_A13**	O	–	**DDR Address Bus [13:0]**
C10	**DDR_A12**	O	–	
B10	**DDR_A11**	O	–	
C11	**DDR_A10**	O	–	
B11	**DDR_A9**	O	–	
A11	**DDR_A8**	O	–	
A12	**DDR_A7**	O	–	
B12	**DDR_A6**	O	–	
A13	**DDR_A5**	O	–	
C13	**DDR_A4**	O	–	
C12	**DDR_A3**	O	–	
B13	**DDR_A2**	O	–	
B14	**DDR_A1**	O	–	
A14	**DDR_A0**	O	–	
C6	**DDR_ODT1**	O	–	**DDR On-Die Termination 1** It is used for On-Die Termination enable of DDR SDRAM device(s) connected to DDR_CS1.
B7	**DDR_ODT0**	O	–	**DDR On Die Termination 0** It is used for On-Die Termination enable of DDR SDRAM device(s) connected to DDR_CS0.
G17	**DDR_DM3_N**	I/O	–	**DDR Data Mask, UDM/LDM** *Note: The operational state is Active-low.*
D18	**DDR_DM2_N**	I/O	–	
E1	**DDR_DM1_N**	I/O	–	
A3	**DDR_DM0_N**	I/O	–	
G18	**DDR_DQS3_T**	I/O	–	**Data Strobe for DQ Lines [DQ24 - DQ31]**
F18	**DDR_DQS3_C**	I/O	–	**Complementary Data Strobe for DQ Lines [DQ24 - DQ31]** *Note: The operational state is Active-low.*
B18	**DDR_DQS2_T**	I/O	–	**Data Strobe for DQ Lines [DQ16 - DQ23]**
C18	**DDR_DQS2_C**	I/O	–	**Complementary Data Strobe for DQ Lines [DQ16 - DQ23]** *Note: The operational state is Active-low.*
G1	**DDR_DQS1_T**	I/O	–	**Data Strobe for DQ Lines [DQ8 - DQ15]**
F1	**DDR_DQS1_C**	I/O	–	**Complementary Data Strobe for DQ Lines [DQ8 - DQ15]** *Note: The operational state is Active-low.*

Table 14 DDR-SDRAM Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
C1	**DDR_DQS0_T**	I/O	–	**Data Strobe for DQ Lines [DQ0 - DQ7]**
B1	**DDR_DQS0_C**	I/O	–	**Complementary Data Strobe for DQ Lines [DQ0 - DQ7]** *Note: The operational state is Active-low.*
A7	**DDR_BG1**	O	–	**DDR4: Bank/Group Address [1];** DDR3: A14
C8	**DDR_BG0**	O	–	**DDR4: Bank/Group Address [0]** DDR3: Bank Address [2]
A8	**DDR_BA1**	O	–	**DDR Bank Address [1]**
A6	**DDR_BA0**	O	–	**DDR Bank Address [0]**
A5	**$\overline{\text{DDR\_CS0}}$**	O	–	**DDR Chip Select 0** *Note: The operational state is Active-low. Use this Chip Select, when only one set of DDR device(s) is connected.*
B6	**$\overline{\text{DDR\_CS1}}$**	O	–	**DDR Chip Select 1** *Note: The operational state is Active-low.*
A9	**DDR_CK_T**	O	–	**DDR Clock Output**
A10	**DDR_CK_C**	O	–	**Complementary DDR Clock** *Note: The operational state is Active-low.*
D7	**DDR_CKE1**	O	–	**DDR Clock Enable 1** It is used for clock enable of DDR SDRAM device(s) connected to DDR_CS1.
C7	**DDR_CKE0**	O	–	**DDR Clock Enable 0** It is used for clock enable of DDR SDRAM device(s) connected to DDR_CS0.
F9	**DDR_ACT_N**	O	–	**DDR4: DDR CMD ACTIVATE** DDR3: A15 *Note: The operational state is Active-low for DDR_ACT_N.*
E7	**DDR_ZQ**	AI	A	**DDR Calibration Resistor**
D12	**DDR_RST**	O	–	**DDR Reset** *Note: The operational state is Active-low for DDR_ACT_N.*
G8	**DDR_PAR**	O	–	**DDR4: DDR Parity**
F8	**DDR_ALERT_N**	O	–	**DDR4: DDR4 ALERT_N** *Note: The operational state is Active-low.*
E12	**DDR_ATO**	AO	A	**Internal Testing** Reserved. Leave it open on PCB.
G12	**DDR_DTO1**	O	–	**Internal Testing** Reserved. Leave it open on PCB.
F11	**DDR_DTO0**	O	–	**Internal Testing** Reserved. Leave it open on PCB.

2.3.11 Reset Signals

Table 15 describes the reset signals.

Table 15 Reset Signals

Ball No.	Name	Pin Type	Buffer Type	Function
K2	**$\overline{\text{POR}}$**	I	PU	**Power-on-Reset Input** *Note: The operational state is Active-low.*
K3	**$\overline{\text{HRST}}$**	O	OD	**Hardware Reset/Power-on-Reset Output** This pin is the POR module output and synchronous with the on-chip reset after power-on. *Note: The operational state is Active-low.*

2.3.12 Power Supply

The power supply characteristics are described in the Electrical Characteristics chapter.

Table 16 Power Supply

Ball No.	Name	Pin Type	Buffer Type	Function
PLL Supply				
R9	**VAA1V8_PLL5**	PWR	–	**High analog power supply for PLL5, PLL2**
R5	**VAA1V8_PLL**	PWR	–	**High analog power supply for PLL3, PLL0a, PLL0b**
K17	**VAA1V8_XO**	PWR	–	**High analog power supply for XO**
J5	**VAA1V8_PVT_L**	PWR	–	**High analog power supply for PVT in Left Side**
L15	**VAA1V8_PVT_R**	PWR	–	**High analog power supply for PVT in Right Side**
P10	**VAA0V9_PLL5**	PWR	–	**Low analog power supply for PLL5, PLL2**
P6	**VAA0V9_PLL**	PWR	–	**Low analog power supply for PLL3, PLL0a, PLL0b**
Digital Supply				
H4, H5	**VDD_IO_0**	PWR	–	**Power supply for digital I/O**
N14, N15	**VDD_IO_1**	PWR	–	**Power supply for digital I/O**
M14	**VDD_IO_2**	PWR	–	**Power supply for digital I/O**
N9	**VDD_IO_3**	PWR	–	**Power supply for digital I/O**
G5, G11, G14, H7, H9, H10, H12, H14, J8, J11, J13, K7, K12, K14, L8, L11, L13, M7, M9, M10, M12	**VDD0V9**	PWR	–	**Digital core power supply** Digital core power supply
Serdes Supply				
L6, M6	**VAA0V9_SPHY1**	PWR	–	**Low analog power supply for SFP Connector Side SerDes**
P12	**VAA0V9_SPHY2**	PWR	–	**Low analog power supply for WAN SerDes**

Table 16 Power Supply (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
K5, M5	**VAA1V8_SPHY1**	PWR	–	**High analog power supply for SFP Connector Side SerDes**
P11	**VAA1V8_SPHY2**	PWR	–	**High analog power supply for WAN SerDes**
DDR Supply				
F7	**VAA1V8_DDRPLL_0**	PWR	–	**Analog power supply for DDR PLL**
F10	**VAA1V8_DDRPLL_1**	PWR	–	**Analog power supply for DDR PLL**
F12	**VAA1V8_DDRPLL_2**	PWR	–	**Analog power supply for DDR PLL**
D4, D6, D13, D15, E5, E6, E8, E11, E13, E14, F4, F15	**VDDQ**	PWR	–	**Power for DDR** 1.5/1.35/1.2 V
G9	**DDR_VREFCA**	PWR	–	**VREF for Command/Address**
G6	**DDR_VREFDQ0**	PWR	–	**VREF for DQ Lines [DQ0 - DQ15]**
G13	**DDR_VREFDQ1**	PWR	–	**VREF for DQ Lines [DQ15 - DQ31]**
OTP Supply				
P4	**VAA1V8_OTP**	PWR	–	**Analog power supply for OTP**

2.3.13 Ground

The power/ground supply characteristics are described in the **Electrical Characteristics** chapter.

Table 17 Ground

Ball No.	Name	Pin Type	Buffer Type	Function
Ground Supply				
J18, K16	**VSSA_XO**	GND	–	**Ground for XO**
K1, K6, L2, L5, M2, M4, N1, N5, N6, P2, R2, T1, T2	**VSSA_SPHY1**	GND	–	**Ground for SFP Connector Side SerDes** Ground
R10, R11, R13, R14, T9, T12, T15	**VSSA_SPHY2**	GND	–	**Ground for WAN SerDes** Ground
A2, A18, B5, B9, B15, C4, C5, C14, C15, D3, D5, D8, D11, D14, D16, E4, E9, E10, E15, F5, F6, F13, F14, G4, G7, G10, G15, H1, H6, H8, H11, H13, H15, H18, J4, J6, J7, J9, J10, J12, J14, J15, J17, K8, K9, K10, K11, K13, L7, L9, L10, L12, L14, L16, M8, M11, M13, M15, M16, M17, M18, N4, N10, N11, N12, N13, N16, P5, P9, P13, P14, P15, R4, R6, R15, T18	**VSS**	GND	–	**Ground** Ground for digital core, I/O logic.

2.3.14 Dying Gasp

Table 18 describes how the dying gasp pin must be connected.

Table 18 Dying Gasp

Ball No.	Name	Pin Type	Buffer Type	Function
K15	**VDD_DG**	PWR	–	**Dying Gasp Reference Input** Input for system supply voltage supervision. This pin is connected to an external system reference voltage to detect a system power failure and to enforce a dying gasp PLOAM message in upstream direction.

2.3.15 Reserved Signals

Table 19 describes how the reserved pins must be connected.

Table 19 Reserved Signals

Ball No.	Name	Pin Type	Buffer Type	Function
J16	**Reserved**	MCL	–	**Tie to VSS**

2.4 Digital Signal Ball (Pin) Reset Property and Drive Strength

This section describes the reset values and drive strength of the digital IO pins.

Table 20 lists the abbreviations used on the following pages.

- The **Reset State** is the logic level of a pin during the power-on-reset (POR) phase.
- The **Reset Release State** is the logic level of a pin after the POR signal transition from low to high.

Table 20 Abbreviations for the Reset Property

Abbreviation	Description
0	Output level Vol, no internal pull-up or pull-down
0-D	Output level Vol, internal pull-down
1	Output level Voh, no internal pull-up or pull-down
1-U	Output level Voh, internal pull-up
Z	High impedance
L	Pin not driven, internal pull-down
H	Pin not driven, internal pull-up

2.4.1 Reset Property and Drive Strength of Peripherals and General Purpose I/O

Table 21 lists the reset property and drive strength of peripherals and general purpose I/O pins.

Table 21 Reset Property and Drive Strength of GPIO Signals

Ball	Name	Reset State	Reset Release State	Drive Strength	Voltage Domain
N18	GPIO0/QSCK	H	H	Default 2 mA, programmable (2, 4, 8, 12 mA): Boot code change the drive strength of the corresponding boot interface to 8 mA.	VDD_IO_2
N17	GPIO1/QSCS	H	H		
P18	GPIO2/QSIO0	H	H		
P17	GPIO3/QSIO1	H	H		
R18	GPIO4/QSIO2	H	H		
R17	GPIO5/QSIO3	H	H		
P16	GPIO8	H	H		VDD_IO_1
T3	GPIO10/I2C1_SCL	H	H		VDD_IO_3
R3	GPIO11/I2C1_SDA	H	H		
T17	GPIO13	H	H		VDD_IO_1
T16	GPIO15	H	H		
R16	GPIO16	H	H		
N8	GPIO20/OPT_RX_LOS	H	H		VDD_IO_3
P8	GPIO21/OPT_TX_DIS_SFP	H	H		
N7	GPIO22/OPT_TX_FAULT	H	H		
P7	GPIO23/OPT_TX_SD	H	H		
R8	GPIO24/OPT_TX_PUP	H	H		
T8	GPIO25/OPT_RX_SD_SFP	H	H		
R7	GPIO26/I2C0_SCL	H	H		
T7	GPIO27/I2C0_SDA	H	H		
T5	GPIO28/GPC1	H	H		
T4	GPIO29/PPS	H	H		
N3	GPIO30/URXD1/URXD1_PON/URXD_TEP/ URXD_QOS/URXD0_PON	H	H		
P3	GPIO31/UTXD1/UTXD1_PON/UTXD_TEP/ UTXD_QOS/UTXD0_PON	H	H		

2.4.2 Reset Property and Drive Strength of UART0 Signals

Table 22 lists the reset property and drive strength of UART0 signals.

Table 22 Reset Property and Drive Strength of UART0 Signals

Ball	Name	Reset State	Reset Release State	Drive Strength	Voltage Domain
J2	URXD0/URXD_QOS/URXD0_PON /URXD1_PON/URXD_TEP	Z	Z	NA	VDD_IO_0
J1	UTXD0/UTXD0_QOS/ UTXD0_PON/UTXD1_PON/ URXD_TEP	H	1	Default 8 mA, programmable (2, 4, 8, 12 mA)	

2.4.3 Reset Property and Drive Strength of Reset Signals

Table 23 lists the reset property and drive strength of reset signals.

Table 23 Reset Property and Drive Strength of Reset Signals

Ball	Name	Reset State	Reset Release State	Drive Strength	Voltage Domain
K2	POR	H	H	NA	VDD_IO_0
K3	HRST	0	H	Default 8 mA, programmable (2, 4, 8, 12 mA)	

2.4.4 Reset Property and Drive Strength of OPT_TXEN Signal

Table 24 lists the reset property and drive strength of OPT_TXEN signals.

Table 24 Reset Property and Drive Strength of OPT_TXEN Signal

Ball	Name	Reset State	Reset Release State	Drive Strength	Voltage Domain
T6	OPT_TXEN	Z	Z	Default 8 mA, programmable (2, 4, 8, 12 mA)	VDD_IO_3

2.4.5 Reset Property and Drive Strength of JTAG Signals

Table 25 lists the reset property and drive strength of JTAG signals.

Table 25 Reset Property and Drive Strength of JTAG Signals

Ball	Name	Reset State	Reset Release State	Drive Strength	Voltage Domain
J3	TRST	H	H	NA	VDD_IO_0
K4	TDI	H	H	NA	
L3	TDO	L	0	Default 8 mA, programmable (2, 4, 8, 12 mA)	
M3	TMS	H	H	NA	
L4	TCK	Z	Z	NA	

2.5 Strap Pin Configuration

Strap pins are used to latch in the system specific configuration after reset. All these pins are input during reset. Table 26 describes the implemented strap on functions and the modes. In addition, there is one more boot strapping to select JTAG mode via TDO pin boot option.

Table 26 Strap Pin Overview

Strap Pin	Function	Description
TDO	JTAG Mode Select	This pin is latched in after reset to define the JTAG interface. Default internal Pull-down. 0_D **Reserved** Used for internal purposes only. 1_D **JTAG** JTAG test mode.
GPIO13	Endian Mode Select	This pin is latched in after reset to define the Endian setting. Default internal Pull-up. 0_D **Little** CPU operates in Little Endian format. 1_D **Big** CPU operates in Big Endian format.
GPIO15	1.8V Supply Select	This pin is latched in after reset to define the power supply for flash interface. Default internal Pull-up. 0_D **1V8** Flash interface power supply is 1.8 V. 1_D **3V3** Flash interface power supply is 3.3 V.
GPIO1 and GPIO0, GPIO16, GPIO31, UTXD0	Boot Select	See Table 44. Default internal Pull-up. Boot select bit 0 is determined by a logical AND of GPIO1 and GPIO0. When any one of the pin strapping on these two pins is low, boot select bit 0 is low. When both of the pin strapping on these two pins are high, boot select bit 0 is high.

3 Data Path

This chapter describes the fast path data flow and the CPU path data flow.

3.1 Data Path Components

Data Path includes these modules:

- One instance of **WAN SerDes** (**Section 4.2**)
- One instance of **XFI SerDes** (**Section 4.3**)
- Two instances of **Ethernet Physical Coding Sublayer** (**Chapter 5**)
- Two instances of **Ethernet MAC** (**Chapter 6**)
- One instance of **PON Subsystem** (**Chapter 7**)
- One instance of **Packet Switching Engine** (**Chapter 8**)
- One instance of **Buffer Manager** (**Chapter 9**)
- One instance of **Carrier Grade Quality of Service Engine** (**Chapter 10**)

3.2 Data Path Flow

Figure 4 shows the data path flow of one PRX126 configuration.

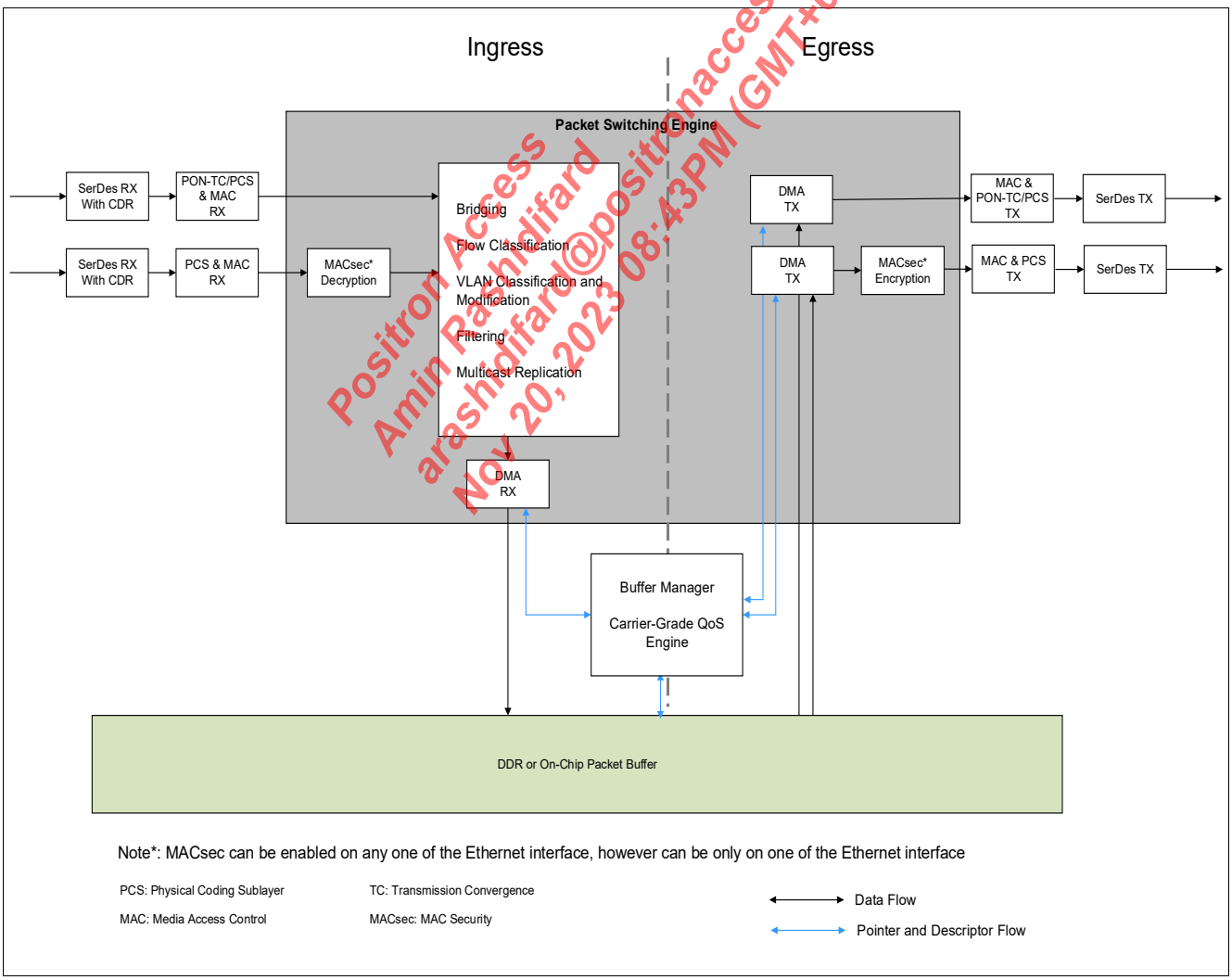


Figure 4 PRX126 Data Path Flow

The data path processes the data traffic between the WAN (PON, AON, or copper wire) interface, also called line interface, and the SFP connector side interface (XFI/SFI/SGMII etc.), also called system interface.

At the WAN side, the device connects to an external optical transceiver or an external Ethernet transceiver seamlessly via a WAN SerDes interface. The PON, AON, or copper wire mode is configurable.

In PON mode, Ethernet packets are received or transmitted through PON TC and the MAC processing module. In either AON or copper wire mode, Ethernet packets are received or transmitted through the Ethernet PCS and MAC processing module.

At the SFP connector side, the interface supports XFI/SFI or SGMII mode.

3.2.1 Fast Path Data Flow

Most of the traffic is processed by the hardware modules without the CPU involvement and follows the fast path data flow. There are the following combinations of the data path flow.

- For the traffic from the line interface to the system interface, when the system interface egress bandwidth is higher than the line interface ingress bandwidth and egress shaping is not applied, the traffic is configured to take **Short-cut Data Path Flow**.
- For the traffic from the line interface to the system interface or the system interface to the line interface, the traffic is configured to take **Full QoS Data Path Flow Ingress** followed by **Full QoS Data Path Flow Egress**.

Short-cut Data Path Flow

The traffic from the line interface to the system interface is enabled to follow the shortcut data path flow as below.

This shortcut path must only be applied when the egress port interface rate is >= the ingress port interface rate and the egress rate shaping is not enabled.

The corresponding data path flow is:

1. Data stream is received and recovered by the line side SerDes. The SerDes converts the serial data stream to a parallel data stream and forwards the data to the Ethernet PCS or the PON TC module.
2. The Ethernet PCS or the PON TC module decodes the data and retrieves the Ethernet packet from the data stream.
3. The received Ethernet packet is forwarded to the packet switching engine directly by the MAC module.
4. When the MACsec function is enabled, the packet is decrypted first before being processed by the Packet switching engine.
5. The packet switching engine parses the packet, bridges, classifies and filters the packet according to the multi-fields of the packet, determines the packet's destinations and characteristics (color and QoS class mapping) based on the classification results. VLAN fields, DSCP field and IP checksum field may be modified according to the classification results. If there are multiple destinations, the packet is replicated for each destination. The copy for each destination can be modified differently.
6. The packet is stored in the shared buffer inside the packet switching engine.
7. When the egress interface indicates that it is ready to accept the next packet, the DMA inside the packet switching engine fetches the packet from the packet switching engine shared buffer and forwards the packet to the egress interface.
8. When the MACsec function is enabled, the packet is encrypted.
9. The transmitted Ethernet packet is forwarded to the Ethernet PCS by the MAC module.
10. The Ethernet PCS does the line encoding/framing and forwards the encoded stream to the system side SerDes.
11. The SerDes converts the parallel data stream to a serial data stream and transmits the data stream.

Full QoS Data Path Flow Ingress

The traffic from the system interface or the line interface follows the Full QoS data path flow ingress part as below.

1. The Ethernet packet is received and recovered by the SerDes. The SerDes converts the serial data stream to a parallel data stream and forwards the data to the Ethernet PCS or the PON TC module.
2. The Ethernet PCS or the PON TC module decodes the data and retrieves the Ethernet packet from the data stream.
3. The received Ethernet packet is forwarded to the packet switching engine directly by the MAC module.
4. When the MACsec function on the Ethernet interface is enabled, the packet is decrypted first before being processed by the Packet switching engine.
5. The Packet switching engine parses the packet, bridges, classifies and filters the packet according to the multi-fields of the packet, determines the packet destinations and characteristics (color and QoS class mapping) based on the classification results. VLAN fields, DSCP field and IP checksum field may be modified according to the classification results. When there are multiple destinations, the packet is replicated for each destination. The copy for each destination can be modified differently.
6. The DMA inside the Packet switching engine requests the free buffer from the Buffer manager.
7. The buffer manager manages both on-chip packet buffer and off-chip packet buffer. The on-chip packet buffer has 7 Mbits. According to the configured buffer allocation policy for each traffic flow and QoS class, the buffer manager allocates the on-chip packet buffer first when it is available and otherwise allocates the off-chip packet buffer.
8. The DMA inside the packet switching engine writes the modified Ethernet packet to the allocated packet buffer.
9. After the DMA stores the complete packet, the buffer manager inserts the packet (via packet pointer and meta QoS information) to the corresponding egress queue managed by the QoS Engine.
10. The carrier-grade QoS engine determines if to enqueue or drop the packet according to the configured RED/WRED policies.

Full QoS Data Path Flow Egress

The traffic to line or system interface follows the Full QoS data path flow egress part as below.

1. The egress interface indicates if it is ready to accept the new packet.
2. When yes, the carrier-grade QoS engine does the rate shaping and schedules the packet from the egress queues mapping to that egress interface.
3. The buffer manager de-queues the packet and passes the packet buffer pointer and the meta information to the DMA inside the Packet switching engine.
4. The DMA inside the Packet switching engine fetches the packet from on-chip or off-chip packet buffer and forwards it to the egress processing modules.
5. After the DMA completes fetching, the buffer manager returns the packet buffer to the free pool.
6. When the MACsec function on the line interface is enabled, the packet is encrypted.
7. The transmitted Ethernet packet is forwarded to the Ethernet PCS or the PON-TC by the MAC module.
8. The Ethernet PCS or the PON-TC does the line encoding/framing and forwards the encoded stream to the system side SerDes.
9. The SerDes converts the parallel data stream to a serial data stream and transmit the data stream.

3.2.2 CPU Path Data Flow

Even though most of the traffic is processed by the hardware modules without the CPU involvement, some control packets, for example, IGMP packets, OAM packets, and PTP packets must be processed by the CPU.

There are two parts in the CPU path data flow.

- CPU ingress: traffic flow from the system or the line interface to CPU
- CPU egress: traffic flow from CPU to the system or the line interface

CPU Ingress Data Flow: from system/line Interface to CPU

The traffic from the line or the system interface is forwarded to CPU for processing. **Figure 5** shows three supported ways based on processing requirements.

1. First way, according to the configurations in the Packet switching engine, the destination port is CPU. The packet is modified according to the configuration associated with CPU as the destination port. The traffic is forwarded to the QoS queues of the CPU port.
2. Second way, according to the configurations in the Packet switching engine, the destination port is a system/line port, however the packet is classified to be extracted before egress queuing to the CPU, the packet is modified according to the configuration associated with the system/line port as the destination port. The traffic is forwarded to the QoS queues of the CPU port. In the meta information of the packet, the original system/line destination port (including GEM port) is provided to the CPU.
3. Third way, according to the configurations in the packet switching engine, the destination port is the system/line port, however the packet is classified to be extracted after egress queuing to the CPU, the packet is modified according to the configuration associated with the system/line port as the destination port. The traffic is forwarded to the QoS queues of the original system/line port. After the buffering/shaping/scheduling of QoS of the original system/line destination port, the traffic is forwarded to the original destination port. However instead of transmitting the packet out, the packet is forwarded to the QoS queues of the CPU port. The packet switching engine may modify the packet payload (for example, time stamp or the counter field in the Ethernet OAM packet) before queuing it to the CPU port. In the meta information of the packet, the original system/line destination port (including GEM port) is provided to the CPU. This path is mainly for Ethernet OAM (e.g. UNI Up MEP) delay and loss measurement. The delay and loss incurred with the egress queuing is accurately measured.

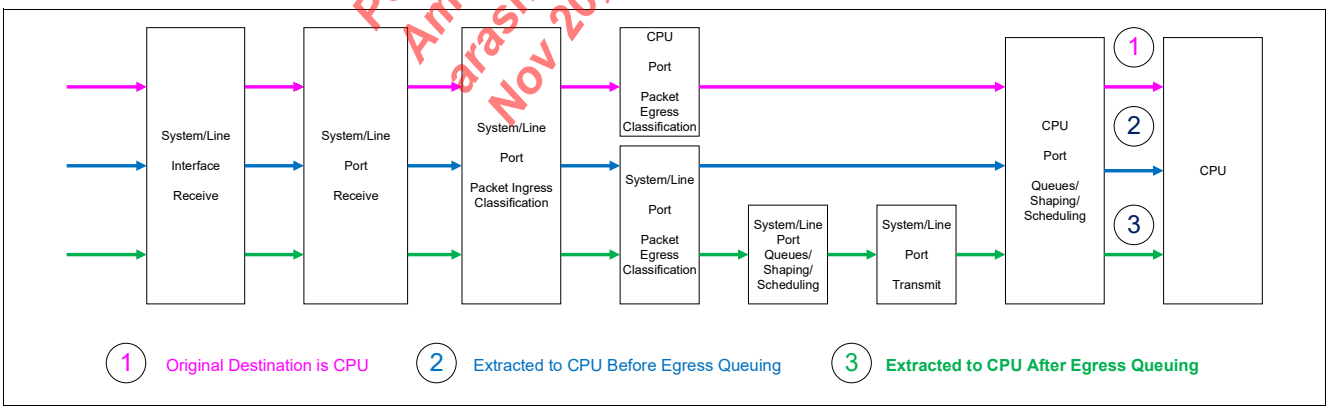


Figure 5 CPU Ingress Data Flow: From System/Line Interface to CPU

The CPU follows the following steps to retrieve the packet from its QoS queues.

1. The CPU gets the packet pointer and the meta information from the load spreader in the buffer manager.
2. When the CPU terminates the packet, after the CPU finishes processing the packet, it returns the buffer pointer to the buffer manager and the buffer manager returns the buffer to the free pool.
3. The CPU may also process the packet, determine the new destination and modify the packet by updating only the header of the packet in the packer buffer. The CPU inserts the packet to the egress queues of the destination. See **Figure 6** for details.

CPU Egress Data Flow: from CPU to System/Line Interface

The traffic from CPU is forwarded to the line or system interface. **Figure 6** shows two supported ways based on processing requirements.

1. First way, the CPU processes the packet and determines the final destination. The traffic is forwarded to the QoS queues of the system/line port. Even in this path, the hardware module (system/line port transmit) inside the packet switching engine may modify the packet payload (for example, time stamp or the counter field in the Ethernet OAM packet) before transmitting it to the interface.
2. Second way, the CPU does not process or only partially processes the packet, inserts the packet to the hardware data path so that the hardware modules process the packet. The CPU queues the packet to the QoS queues dedicated for CPU insertion. The meta information in the description carries the original source system/line port (including GEM port). The packet switching engine does the ingress packet classification according to the configuration associated with the original system/line port.

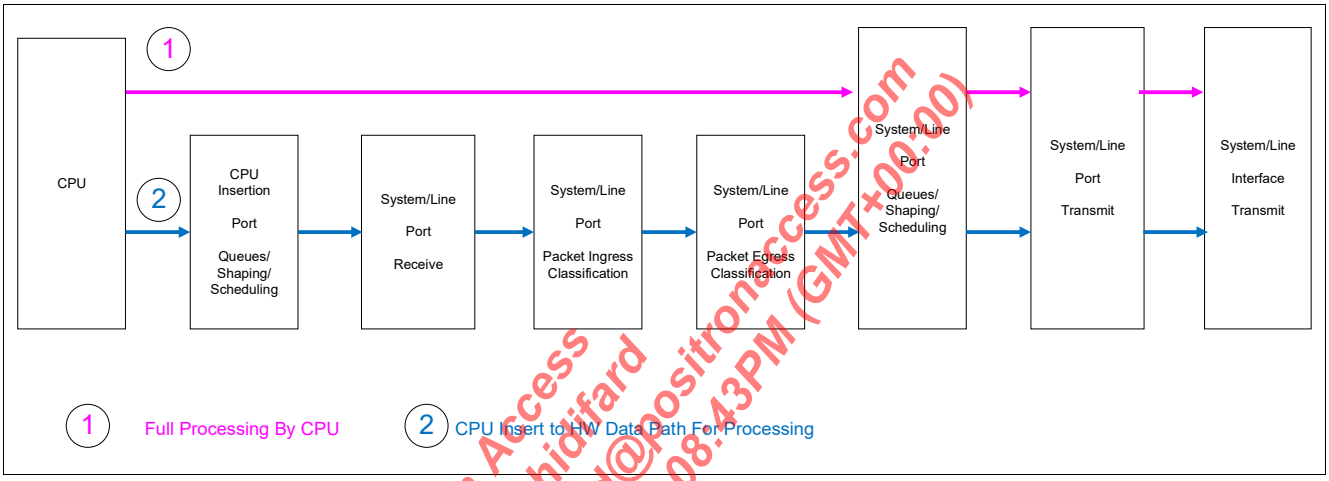


Figure 6 CPU Egress Data Flow: From CPU to System/Line Interface

The CPU follows the following steps to insert the packet to the QoS queues.

1. The CPU writes the packet pointer and the meta information to the buffer manager.
2. The buffer manager inserts the packet, via packet pointer and meta information for QoS, to the egress queue managed by the QoS Engine.

Multi-core Processing Engine Path

The packet switching engine extracts the data packets that require advanced or complementary processing (for example, routing, tunneling, L2NAT etc) to MPE. The packets are stored in the egress queues dedicated to MPE. The data path is the same as shown in **Figure 5** and **Figure 6**.

For the traffic to MPE, the packet switching engine attaches the packet parsing information before the start of the packet in order to reduce the MPE processing load.

See **Multi-core Processing Engine** for the offloading capability description.

4 SerDes

PRX126 supports two SerDes instances.

- One SerDes (WAN SerDes) is for line side
- One SerDes (XFI SerDes) is for system side (SFP connector side)

4.1 SerDes Instances

Figure 7 shows the SerDes instances overview. The MAC number starts from 2.
Number 0 and 1 are reserved for pseudo MAC interfaces connecting to DMA inside packet switching engine.

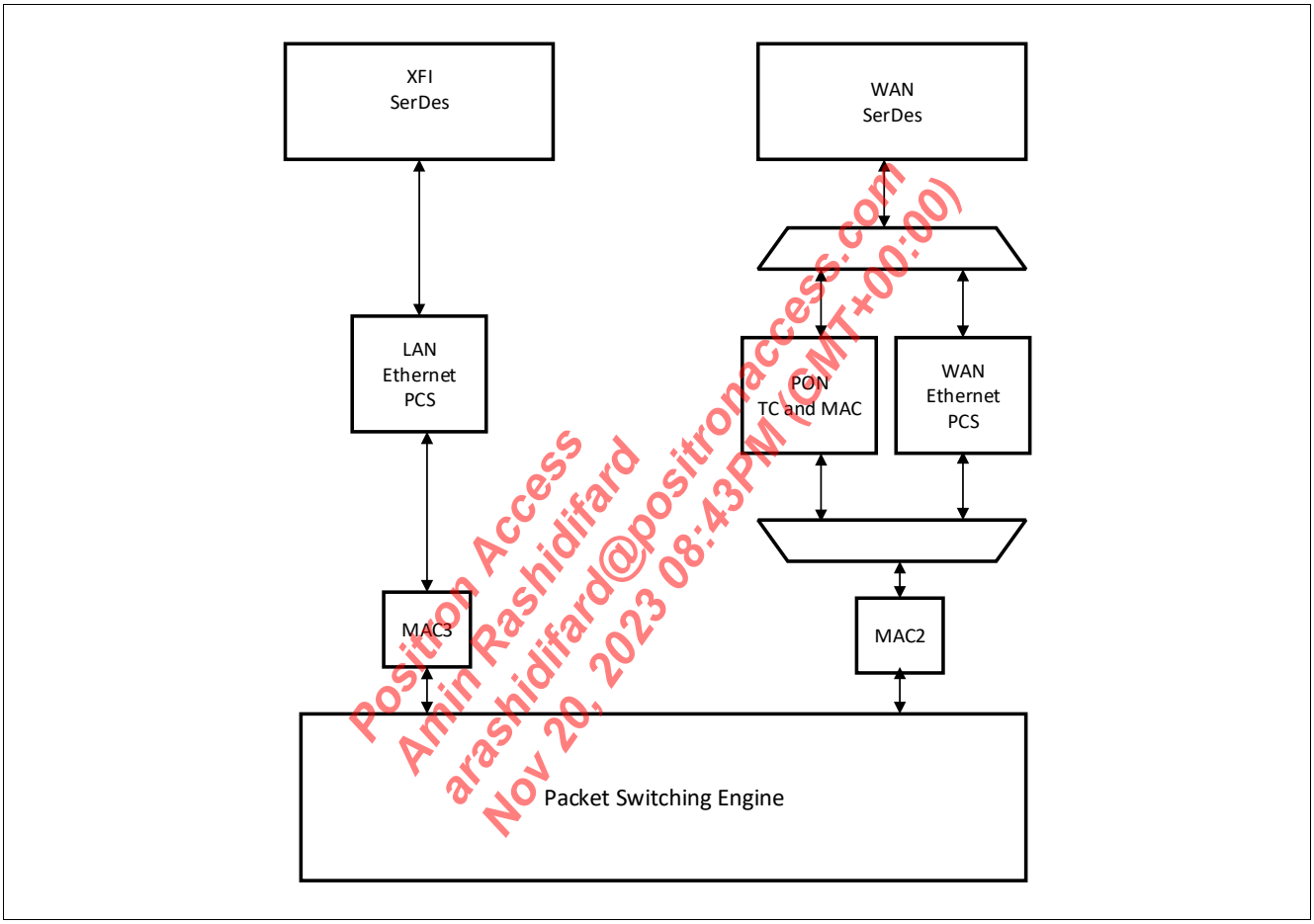


Figure 7 SerDes Instances

4.2 WAN SerDes

The SerDes in WAN side is either connected to an external optical transceiver in PON mode as ONU, an external optical transceiver in AON mode or an external BASE-T Ethernet transceiver in copper wire mode.

The WAN SerDes supports the following features.

- Single lane
  - A high speed differential transmit pair
  - A high speed differential receive pair
  - An external reference resistor for calibration of TX and RX termination
- PON mode with an external optical transceiver
  - GPON (RX: 2.48832 Gbit/s and TX: 1.24416 Gbit/s) **[9]**
  - XG-PON (RX: 9.95328 Gbit/s and TX: 2.48832 Gbit/s) **[10]**

  - NG-PON2 (RX: 9.95328 Gbit/s and TX: 9.95328 Gbit/s) [11]
  - XGS-PON (RX: 9.95328 Gbit/s and TX: 9.95328 Gbit/s) [12]
  - EPON (RX: 1 Gbit/s and TX: 1 Gbit/s) [14]
  - 10G-EPON asymmetric (RX: 10 Gbit/s and TX: 1 Gbit/s) [14]
  - 10G-EPON symmetric (RX: 10 Gbit/s and TX: 10 Gbit/s) [14]
  - Loop clock from RX CDR to TX in PON mode
- AON mode with an external optical transceiver via XFI/SFI [23], 10G-KR [19], or 1000BASE-X [19] SerDes
  - 1000BASE-X
  - 10GBASE-R
- Copper wire mode with an external Ethernet transceiver via XFI/SFI [23], 10G-KR [19], 1000BASE-X [19], 10G single-port USXGMII [22], 1G SGMII [21], or 2.5G SGMII [19] SerDes
  - 10GBASE-T
  - 5GBASE-T
  - 2.5GBASE-T
  - 1GBASE-T
  - 100BASE-TX
  - 10BASE-T(e)
- Transmit and receive equalization and adaption
- TX amplitude control
- Independent RX and TX power state controls
- Supports bit error rate of 1E-12 or better
- Debug support
  - Diagnostics for characterization and ATE testing: loopback, test pattern generation, BERT, error insertion and detection

4.3 XFI SerDes

The SerDes is connecting to the interface at an SFP/SFP+ module.

- The SerDes has single lane
  - A high speed differential transmit pair
  - A high speed differential receive pair
  - An external reference resistor for calibration of TX and RX termination
- Supports and complies the following:
  - 10 Gbit/s XFI/SFI [23] or single-port UXSGMII [22]
  - 2.5 Gbit/s SGMII or 2500BASE-X [19]
  - 1 Gbit/s SGMII [21] or 1000BASE-X [19]
- Transmit and receive equalization and adaption
- TX amplitude control support
- Independent RX and TX power state controls
- Supports Bit Error Rate of 1E-12 or better
- Debug support
  - Diagnostics for characterization and ATE testing: loopback, test pattern generation, BERT, error insertion and detection

5 Ethernet Physical Coding Sublayer

There are two Ethernet physical coding sublayer (PCS) instances in total. They are connected to the WAN SerDes and the SFP side XFI SerDes. The Ethernet PCS supports the following features.

- PCS coding
  - 1000BASE-(K)X with 8b/10b coding (clause 36) [19]
  - 10GBASE-(K)R with 64/66b coding (clause 49) [19]
- Supports clause 73 [19] auto-negotiation
  - 1000BASE-(K)X: 1 Gbit/s (1.25 GT/s)
  - 10G-(K)R: 10 Gbit/s (10.3125 GT/s)
- Supports 10G single-port USXGMII with clause 37 [22] auto-negotiation for the following:
  - Single-port USXGMII is based on 10G-(K)R
  - Speed and duplex modes are auto-determined without software involvement
  - 10 Gbit/s (10.3125 GT/s)
  - 5 Gbit/s (10.3125 GT/s)
  - 2.5 Gbit/s (10.3125 GT/s)
  - 1 Gbit/s (10.3125 GT/s)
  - 100 Mbit/s (10.3125 GT/s)
  - 10 Mbit/s (10.3125 GT/s)
- Supports SGMII [21] or 1000BASE-(K)X with clause 37 [19] auto-negotiation for the following per Ethernet PCS
  - Speed and duplex modes are auto-determined without software involvement
  - 1 Gbit/s (1.25 GT/s)
  - 100 Mbit/s (1.25 GT/s)
  - 10 Mbit/s (1.25 GT/s)
- Supports 2.5 Gbit/s SGMII or 2500BASE-(K)X [19]
  - 2.5 Gbit/s (3.125 GT/s)
- Supports clause 72 [19] for 10G-BASE (K)R training
- Supports clause 74 [19] Forward Error correction and forwarding in 10G-BASE (K)R mode
- Supports EEE low power Idle [19] mode
- Supports both full and half duplex modes in 100/10 Mbit/s speed

6 Ethernet MAC

There are two Ethernet MAC instances in total. They are connected to LAN Ethernet PCS instance and WAN Ethernet PCS instance. Ethernet MAC supports the following features.

- XGMII interface is compliant to IEEE 802.3 Clause 46 [19]
- GMII interface is compliant to IEEE 802.3 Clause 35 [19]
- MII interface is compliant to IEEE 802.3 Clause 22 [19]
- 10/100/1000/2500/5000/10000 Mbps standard operation speed
- Full-duplex operation mode (for all speeds) and half-duplex operation mode (only for 10/100 Mbps standard operation speed)
- Enhanced frame size support (jumbo frames, programmable limit up to 10 Kbyte)
- Pause frame in full duplex mode. Backpressure (forced collisions) in half-duplex mode
- Frame padding on egress traffic
- Minimum frame length check and maximum frame length check. Maximum frame length are configurable.
- FCS verification and stripping
- FCS generation and insertion
- Supports low power idle (LPI) mode as defined by IEEE 802.3az [19]

Ethernet MAC also supports the following PTP/1588 time synchronization features for operation speed 1000 Mbit/s and above.

- Supports Ethernet packet time stamping as IEEE 1588 (v1 and v2), ITU G.8275 and Y.1369
- Supports ordinary clock, boundary clock, end to end transparent clock and peer to peer transparent clock modes
- Supports PTP over Ethernet and PTP over UDP over IPv4/IPv6.
- Supports both external reference time (from PON TC and MAC) and internal reference time. Internal reference time can be time adjusted and frequency adjusted.
- Auxiliary time stamp snapshot with two external events. Support 1 PPS (pulse per second) output.
- Supports both fixed and flexible (programmable for start, stop, pulse width, interval) PPS output.
- Snapshot of packet at SFD in both direction. Support programmable ingress time stamp correction and programmable egress time stamp correction.
- Attaches the captured time stamp to end of the every received packet to CPU
- Supports one step and two step time stamping in TX direction

7 PON Subsystem

The PON subsystem implements the PON related functions of the WAN interface. It resides between the WAN-side Ethernet MAC and the WAN SerDes. The PON interface is designed in a way to allow direct connectivity to a pluggable transceiver SFP/SFP+ or to a PMD transceiver chip (LDD/LA).

Supported PON Modes

- ITU-T G.984 G-PON [9]
- ITU-T G.987 XG-PON [10]
- ITU-T G.9807 XGS-PON [11]
- ITU-T G.989 NG-PON2 [12]
- EPON (1000BASE-PX) [14]
- 10G-EPON (10/1GBASE-PRX, asymmetric) [14]
- 10G-EPON (10GBASE-PR, symmetric) [14]
- Active Ethernet (10GBASE-R, 1000BASE-X)
- Bit/baud rates downstream/upstream:
  - GPON: 2.488 Gbit/s (downstream), 1.244 Gbit/s (upstream)
  - XG-PON: 9.952 Gbit/s (downstream), 2.488 Gbit/s (upstream)
  - XGS-PON: 9.952 Gbit/s (downstream), 9.952 Gbit/s (upstream)
  - NG-PON2: 9.952 Gbit/s (downstream), 9.952 Gbit/s (upstream)
  - EPON: 1 Gbit/s (downstream bit rate), 1 Gbit/s (upstream bit rate), 1.25 GT/s (downstream baud rate), 1.25 GT/s (upstream baud date)
  - 10G-EPON asymmetric: 10 Gbit/s (downstream bit rate), 1 Gbit/s (upstream bit rate), 10.3125 GT/s (downstream baud rate), 1.25 GT/s (upstream baud rate)
  - 10G-EPON symmetric: 10 Gbit/s (downstream bit rate), 10 Gbit/s (upstream bit rate), 10.3125 GT/s (downstream baud rate), 10.3125 GT/s (upstream baud rate)

Dimensioning

- 64 T-CONTs
- A single 8 kHz frame is able to handle at least 32 T-CONTs in XG-PON/XGS-PON mode and 24 T-CONTs in GPON mode, unless stated otherwise in the related SDK release notes.
- 256 GEM or XGEM ports (unicast or multicast)
- Up to 16 LLIDs

Other Characteristics

- Supports SFF/SFP/XFP transceivers, fixed or tunable wavelength
- Configurable burst enable timing
- Integrated voltage supervision and automatic dying gasp insertion
- Automatic power saving control
- ToD counter with capture/compare unit
- Receive and transmit time stamping in ITU modes

Management

- Integrates autonomous PLOAM and MPCP handling to decouple real-time low level control functions from higher layer software tasks
- Functional API and higher layer control protocols like OMCI [13] and SIEPON [16] implemented in software on main CPU under Linux*
- Message-based mailbox communication between PON subsystem and main CPU under Linux*

8 Packet Switching Engine

The packet switching engine subsystem includes the dedicated functions for the L2 bridging data plane and the QoS mapping functions as defined in ITU-T G.988 for ITU based PON systems [13] and SIEPON [16]. The subsystem allows straight-forward mapping from Linux* bridge and follows closely G.988 OMCI and SIEPON packet processing model and BBF TR-156 specification [17].

This chapter provides an overview of the engine. It covers the description of the main features and the subsystem functional description.

8.1 Features

MACsec [24]

- One instance of MACsec
  - Configurable to be attached to only one of MAC instances
- IEEE 802.1AE/AEbn/AEbw. Supports both GCM-AES 128 bit and 256 bit. 16 security channels and 32 security associations in each direction
- Supports classification based on VLAN tag field, Ethernet type and MACsec tag field
- Supports bypassing for non-MACsec packets
- Supports VLAN bypassing
- 10 Gbit/s in-line encryption and decryption

Packet Switching

- Bi-directional 10 Gbit/s wire-speed bridging, VLAN classification and modification, filtering and flow based classification for all valid packet sizes
- Microcode based flexible packet parsing on first 256 bytes of the packet
- 288 CTP ports assignable per GPON GEM port, EPON LLID and Ethernet port
- 128 bridge ports assignable per VLAN rule of each CTP port
- IEEE 802.1D: automatic learning and aging of MAC addresses
  - 64 combinations of L2 bridges and VLANs
- Supports L2 security
  - IEEE 802.1X
  - MAC address learning limitation
  - MAC port locking and MAC table freeze
  - Source MAC address filtering and destination MAC address filtering, both white list and black list modes
- Supports L3 multicast processing and replication at bridge port level
  - Supports 512 IPv4/IPv6 multicast Groups and 64 VLANs
  - Supports any source multicast and source specific multicast
- Supports 1024 entries for VLAN tagging filtering
- Supports 1024 rules for extended VLAN tagging operation
  - Supports four VLAN tag TPID values globally; one TPID value is 0x8100, the other three TPID values are programmable globally
- Supports 512 rules in flexible traffic flow classification based on multiple fields of the packet
- Packet filtering based on multiple fields of the packet
- Traffic QoS mapping classification
- Priority, DSCP and color marking/remarking
- Supports 128 srTCM and trTCM traffic meters with maximum 64KB burst size
- Wake on LAN
- Port trunking of any two ports
- Packet statistics

  - Receive and transmit counters per CTP port and per bridge port
- Packet mirroring
  - Mirroring of ingress traffic, enabled per CTP and per VLAN rule of each CTP
  - Mirroring of egress traffic, enabled per CTP and per VLAN rule of each CTP
- Packet loop-back
  - Ingress loopback, enabled per CTP and per VLAN rule of each CTP
  - Egress loopback, enabled per CTP and per VLAN rule of each CTP
- 802.1ag and Y.1731 Ethernet OAM delay and loss measurement hardware support
- Ethernet OAM loopback support

DMA

- DMA to store the packet to on-chip or off-chip packet buffer
- DMA to fetch the packet from on-chip or off-chip packet buffer
- Request and release the free buffer from/to the buffer manager

8.2 Functional Description

This section provides the detailed functional description of the packet switching engine.

8.2.1 ITU-T G.988 OMCI L2 MAC Bridge Reference Model

The OMCI supports two major layer 2 traffic mapping models: MAC bridging and IEEE 802.1p mapping. MAC bridging is described in [IEEE 802.1D] and [IEEE 802.1Q]. The bridge has many features, and is used to direct traffic based on a MAC address (true bridging) or on VLAN characteristics, using the VLAN filter feature.

The two basic layer 2 services are used in various combinations to achieve different overall connectivities.

- N:1 bridging, where a bridge is used to serve multiple UNI ports from a single ANI service.
- 1:M mapping, where a mapper is used to serve a single UNI with multiple ANI connections, based on IEEE 802.1p priorities.
- 1:P filtering, where a bridge with filters is used to serve a single UNI with multiple ANI connections, based on some VLAN information other than IEEE 802.1p priorities.
- N: MP bridging map filtering, the combination of the above.

8.2.2 ITU-T G.988 OMCI L2 MAC Bridge Implementation

The PRX126 packet switching follows closely the G.988 OMCI packet processing model and offers the flexibility of packet processing options required by the OMCI model and the BBF TR-156 specification **[17]**. The great advantage of the implemented network processing unit is that each attribute of the received OMCI ME is directly mapped to the underlying hardware.

Figure 8 describes the OMCI model implemented by PRX126, where arrows (unlike in OMCI ME relationship diagrams) denote the sequence of packet processing in up- and downstream direction. The number in brackets defines the number of occurrences of that particular instance. The hardware instances of the managed entities support all attributes of the corresponding G.988 defined ME. Depending on the selected OMCI model the corresponding hardware instances are activated.

Bridging is done either in a single bridge or in several bridges. Up to 64 L2 bridges are supported.

- Overall maximum 288 CTP bridge ports are supported (1 of them is reserved for internal processing purpose)
- Overall maximum of 128 bridge ports are supported (1 of them is reserved for internal processing purpose)
- L2 or L3 multicast: L2 multicast is based on the destination MAC address and 64 VLANs; L3 multicast is based on destination, source IP addresses and 64 VLANs.
- Overall maximum 1024 extended VLAN tagging (EVTC) rules are supported and flexibly assigned as indicated in **Figure 8**.
- Overall maximum 1024 VLAN filtering TCI values are supported and flexibly assigned as indicated in **Figure 8**.
- Overall maximum of 128 rate limiters are supported and flexibly assigned as indicated in **Figure 8**.
- Egress priority queue management, shaping and schedule are handled by the **Carrier Grade Quality of Service Engine** outside of the Packet switching engine.

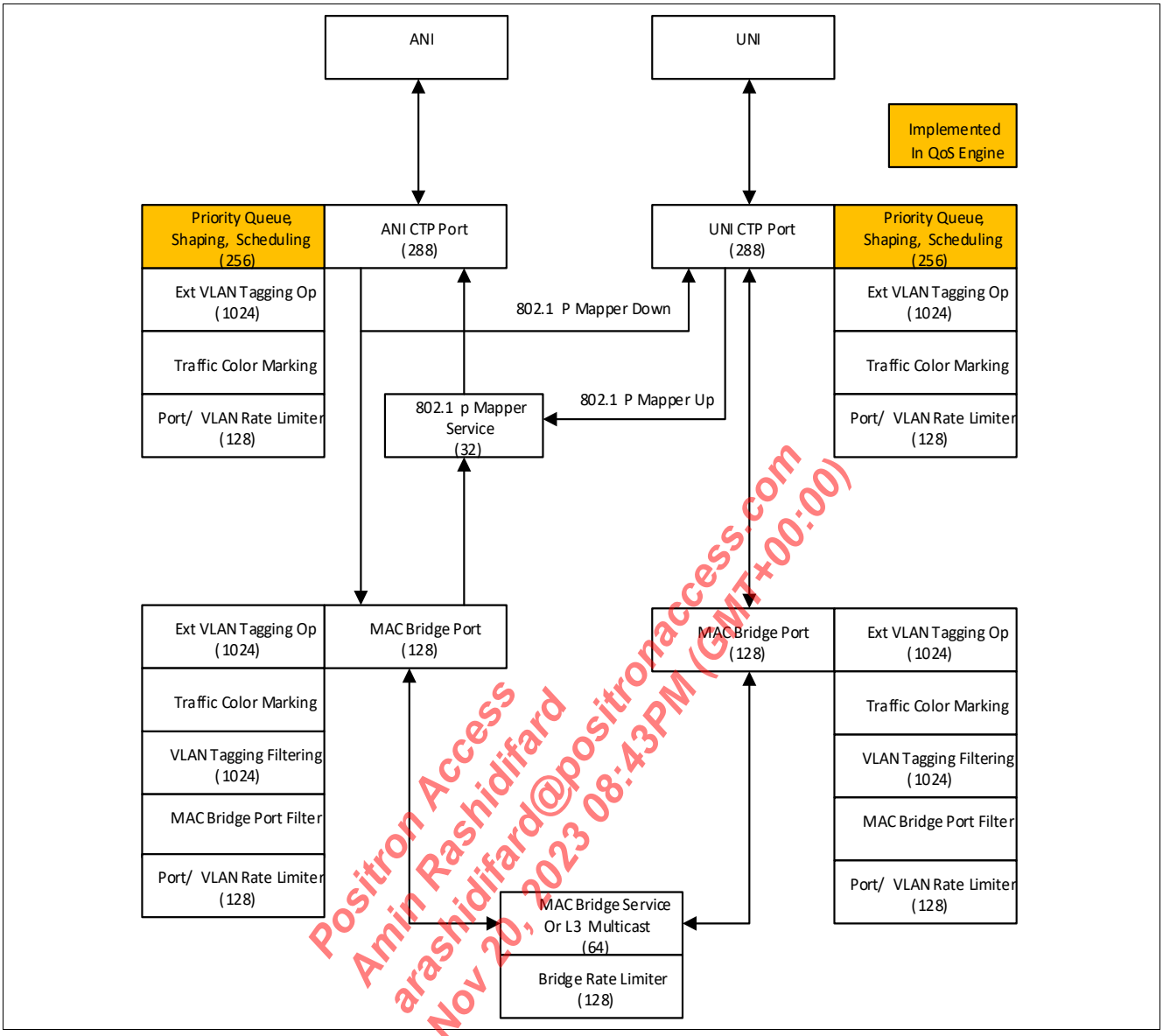


Figure 8 OMCI L2 MAC Bridge Implementation

8.2.3 Traffic Processing Stages

Figure 9 shows the traffic processing stages inside the packet switching engine. There are two major processing parts in the packet switching engine:

- Ingress Classification
  - Ingress classification processing stage is triggered only once.
  - Ingress classification processing stage determines the egress (destination) bridge port list which is either empty or include one destination bridge port or multiple destination bridge ports.
- Egress Classification
  - When the egress bridge port list is empty, the packet is discarded at the end of the ingress classification stage and egress classification stage is skipped.
  - For every member in the egress bridge port list, egress classification processing stage is triggered once.

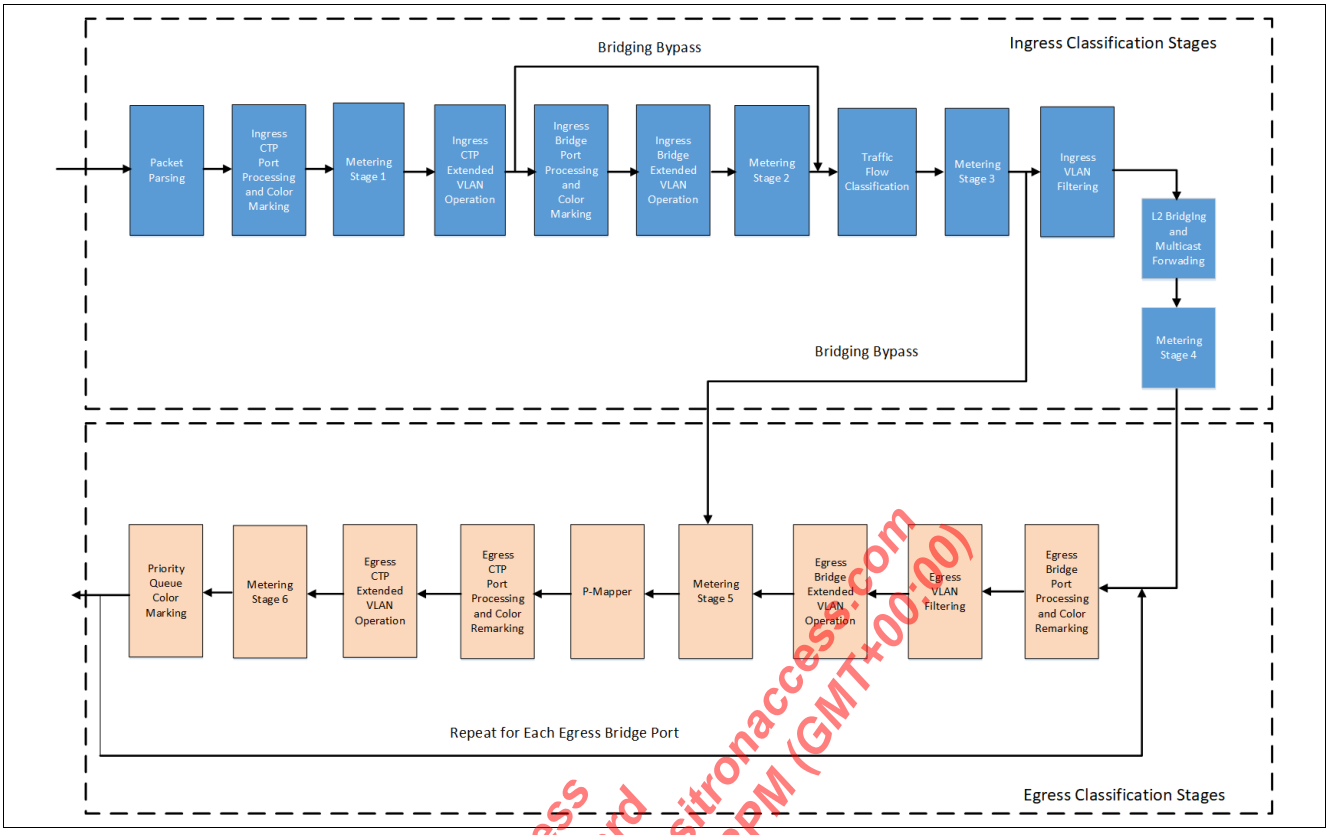


Figure 9 Traffic Processing Stages

Parsing

The parsing feature in the packet switching engine is realized as a microcoded engine. This allows a flexible adaptation to any future protocol changes. The parser microcode evaluates the first 256 bytes of the frame header and is capable of extracting all relevant information up to payload after the layer 4 protocol from the frame. The microcode has to be loaded and enabled, otherwise only the MAC destination and MAC source address are extracted from the packet.

Ingress CTP Port Processing

A CTP Port refers to the GEM port over GPON or LLID over EPON, and the Ethernet port.

When a packet is received, it is classified according to the configurations associated with the ingress CTP port as follows.

- Assigning a bridge port ID
- Assigning a default traffic class
- Assigning enable/disable operation and the entries in the extended VLAN tagging operation table
- When loopback is enabled, determines the destination information. Assigns destination MAC and source MAC swap enable/disable.
- Determining the color according to DSCP field, VLAN PCP and DEI field and ingress color marking mode
- Assigning enable/disable operation and meter ID for metering stage 1
- When bridge bypass mode is enabled, determining the destination information according to the configurations
- Assigning enable/disable operation for ingress mirroring
  – When ingress mirroring is enabled, traffic is forwarded to the monitoring port unchanged.

Ingress CTP Port Extended VLAN Tagging Operation Processing

This stage is only triggered if ingress CTP extended VLAN tagging operation is enabled. Otherwise, this stage is skipped.

The extended VLAN tagging operation table is searched and the action stored in the treatment part of the matched entry is taken.

When the packet is determined to be discarded according to configuration in extended VLAN tagging table, the subsequent processing stages are skipped.

Besides the treatment defined in ITU-T G.988, the following additional treatments are supported by extended VLAN tagging operation.

- Loopback enable/disable and DA/SA swap enable/disable
- Overriding the bridge port with the configuration in the matched entry
- Overriding the traffic class with the configuration in the matched entry
- Mirror enable/disable

Ingress Bridge Port Processing

The bridge port refers to an individual interface at the bridge.

A packet is classified according to configurations associated with the ingress bridge port as follows.

- Assigning a bridge ID
- Assigning the limiting numbers of the source MAC address
- Assigning source MAC address learning enable/disable operation
- Assigning L2 table destination MAC address lookup enable/disable operation
- Assigning L3 multicast IP lookup enable/disable operation
- Assigning enable/disable operation and the entries in the extended VLAN tagging operation table
- Determining the color according to DSCP field, VLAN PCP and DEI field and ingress color marking mode
- Assigning enable/disable operation and meter ID for metering stage 2
- Assigning enable/disable operation, filtering modes and the entries in the ingress VLAN filtering table
- Assigning the filter bridge port member list for all the traffic from this ingress bridge port
  - The traffic are only forwarded to the destination bridge ports which are the members of the ingress bridge port. This allows local switching to be blocked. By clearing the bit in the ingress port bit position, ingress port removal is achieved.
- Assigning ingress spanning tree state

Ingress Bridge Port Extended VLAN Tagging Operation Processing

This stage is only triggered if ingress bridge port extended VLAN tagging operation is enabled. Otherwise, this stage is skipped.

The extended VLAN tagging operation table is searched and the action stored in the treatment part is taken.

When the packet is determined to be discarded according to configuration in extended VLAN tagging table, the subsequent processing stages are skipped.

Traffic Flow Classification Processing

The traffic flow classification table is searched and the action stored in the treatment part is taken. There are 512 entries in the traffic flow classification table. The following actions are taken based on the configurations.

- Overriding the traffic class with configuration in the matched entry
- Overriding the bridge ID with configuration in the match entry
- Overriding the destination bridge port list with configuration in the matched entry. When the bridge port list override action is enabled in the matched entry, meter stages 3, 4, 5 and 6 are skipped.
- Assigning the filter bridge port member list for all traffic. This is used to `and` with the filter bridge port member list from the previous steps and the destination bridge port list determined after L2/L3 forwarding.

- Assigning the filter bridge port member list for unknown traffic. This is used to `and` with the filter bridge port member list from the previous steps and the destination bridge port list determined after L2/L3 forwarding.
- Assigning a color
- Identifying PTP event packets
- Assigning source MAC address learning enable/disable
- Identifying Ethernet OAM packets and Ethernet OAM flow ID
- Assigning extraction enable/disable and modes
- Assigning meter enable/disable and the meter ID for stage 3

Ingress Bridge Port VLAN Filtering Processing

This stage is only triggered if the ingress bridge VLAN filtering is enabled. Otherwise, this stage is skipped.

The VLAN filter table is searched according to the outer VLAN TCI field (modified from the previous stages) and the action stored in the VLAN table is taken.

When the packet is determined to be discarded, the subsequent processing stages are skipped.

L2-Bridging/L3-Multicast Forwarding Processing

This stage is triggered if bridging function is not bypassed.

The MAC bridging table is searched and updated When the SA learning and/or DA lookup is enabled. The multicast table is searched When the multicast IP lookup is enabled.

The following are assigned.

- Destination bridge port list
- Assigning meter enable/disable and corresponding meter ID per bridge for different types of traffic: broadcast, multicast, unknown multicast IP, unknown multicast non-IP, unknown unicast traffic for metering stage 4
- Updating learning discard counter

Egress Bridge Port Processing

The packet is classified according to the configurations associated with the egress bridge port as follows.

- Assigning an egress corresponding CTP port
- Assigning P-mapper enable/disable, P-mapper mapping mode and P-mapper ID
- Assigning extended VLAN tagging operation enable/disable and entires
- Assigning an egress color
- Assigning traffic meter enable/disable and corresponding Meter ID for different types of traffic: broadcast, multicast, multicast IP, multicast non-IP, unknown unicast for meter stage 5
- Assigning an egress Spanning tree state
- Assigning egress VLAN Filtering enable/disable, filtering mode and entries

Egress Bridge Port VLAN Filtering Processing

This stage is only triggered if egress bridge VLAN filtering is enabled. Otherwise, this stage is skipped.

The VLAN filter table is searched according to the outer VLAN TCI field (modified from the previous stages) and the action stored in the VLAN table is taken.

When the packet is determined to be discarded, the subsequent processing stages are skipped.

Egress Bridge Port Extended VLAN Tagging Operation Processing

This stage is only triggered if egress bridge port extended VLAN tagging operation is enabled. Otherwise, this stage is skipped.

The extended VLAN tagging operation table is searched and the action stored in the treatment part is taken. When the packet is determined to be discarded according to configuration in the extended VLAN tagging table, the subsequent processing stages are skipped.

P-Mapper Processing

This stage is only triggered when P-mapper is enabled.

The destination CTP port is assigned.

Egress CTP Port Processing

The packet is classified according to configurations associated with the egress CTP port as follows.

- Assigning extended VLAN tagging operation enable/disable and entries
- When loopback is enabled, override the destination parameters determined by the previous steps
- Assigning an egress color
- Assigning egress color marking mode override enable/disable and marking mode for priority queue
- Assigning traffic meter enable/disable and meter ID for metering stage 6
- Assigning enable/disable operation for egress mirroring
  - When egress mirroring is enabled, traffic is forwarded to the monitoring port with the same modification performed as the packet being mirrored.

Egress CTP Port Extended VLAN Tagging Operation Processing

This stage is only triggered if egress CTP Port extended VLAN tagging operation is enabled. Otherwise, this stage is skipped.

The extended VLAN tagging operation table is searched and the action stored in the treatment part is taken.

When the packet is determined to be discarded according to configuration in the extended VLAN tagging table, the subsequent processing stages are skipped.

Priority Queue Egress Color Marking

The color (to QoS Engine) is marked according to PCP+DEI+DSCP and the egress priority queue color marking mode.

9 Buffer Manager

The buffer manager (BM) is composed of these sub-modules.

- The enqueue manager (EQM) responsible for the assignment of free buffers to the ingress ports and en-queuing the filled buffers into the QoS Engine queues
- The dequeue manager (DQM) responsible for the de-queuing of the buffers from the QoS Engine queue to the egress ports and returning the free buffers to the BM
- The free segment queue manager (FSQM) responsible for the buffer management of the buffers in the internal memory and for the segment linking of the segmented internal packets
- The external buffer manager (EBM) responsible for the packet buffer management of the buffers in the external memory
- The PON-IP interface block (PIB) responsible for taking in requests from the PON TC processing module for de-queuing the required number of packets out for the respective T-CONT
- The load spreader (LS) responsible for spreading the egress traffic towards the CPU

9.1 Buffer Manager Overview

Figure 10 shows the buffer manager architecture.

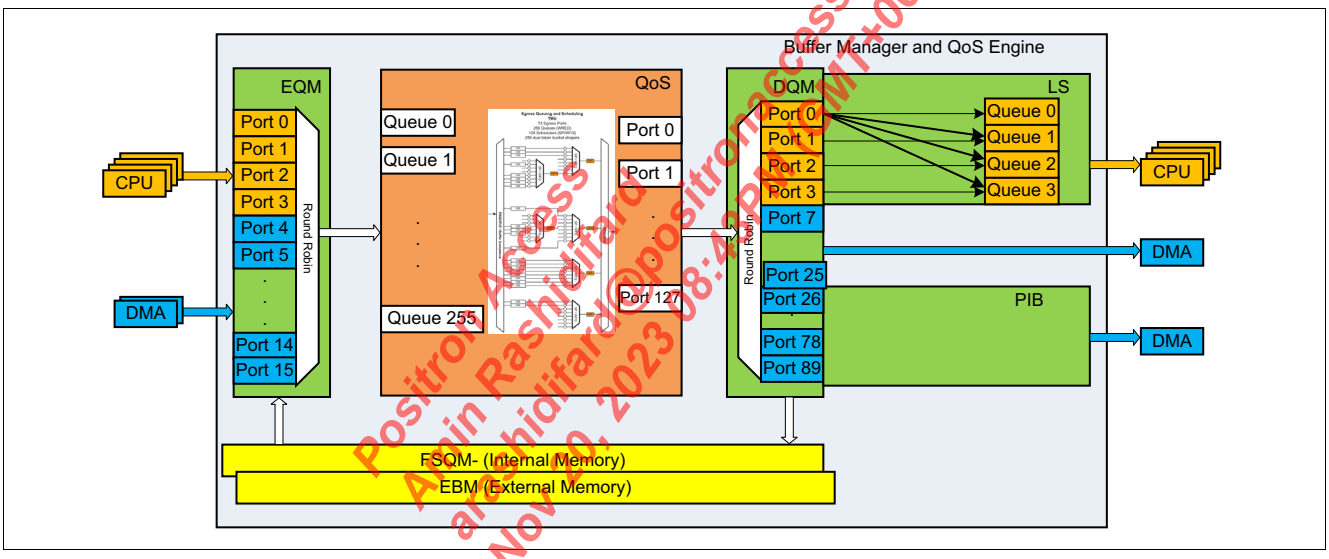


Figure 10 BM and QoS Architecture

The packet is either assigned to the internal packet buffer or to one pool of the external packet buffer according to the buffer allocation algorithm and the packet attributes: packet destination, packet size and packet traffic class.

9.2 Enqueue Manager

The enqueue manager (EQM) supports these configurations:

- CPU ports for 4 VPE
- DMA ports for data path from the packet switching engine

9.3 Dequeue Manager

The dequeue manager (DQM) supports up to 90 ports, comprising of these configurations:

- 4 CPU ports
  - 4 ports for the 4 VPE
- 19 DMA ports for data path to the packet switching engine
- 64 special PON ports (with separate descriptors for segmented and non segmented) for the PON TC module.

9.4 Free Buffer Manager

The free buffer manager provides buffers for the internal memory region and the external memory region.

- Internal memory region with a 7 Mbit on-chip packet buffer: 7k buffer pointers with 128 bytes per buffer. One packet may occupy multiple buffers. This region is managed by FSQM.
- External memory region with off-chip packet buffer: both the packet pointer and buffer are in external memory. One packet occupies one buffer. This region is managed by EBM. 4 pool sizes are supported: 512 Byte, 1 Kbyte, 2 Kbyte, and 10 Kbyte.
- The packet buffer allocation is based on the buffer request of the packet. The allocation is determined by the packet destination, QoS class, packet size, each type of buffer occupancy and the configured watermarks. The internal packet buffer is allocated first in order to reduce the power consumption by external memory interfaces and devices.

9.5 Load Spreader Overview

The load spreader (LS) is a module shared between the dequeue manager (DQM) and the MIPS cluster. The LS has one port towards the MIPS cluster per input port from the dequeue manager.

The LS provides the following basic functions.

- Interrupt based interface for the MIPS processing cluster to read the descriptors for the software or MPE processing
- Configurable load spreading of the traffic directed towards the CPU port
- A FIFO based mechanism for fetching multiple descriptors with single interrupt request for faster and simplified CPU performance
- Threshold and timer based interrupts for CPU
- Depending on their own processing the virtual CPUs of the MIPS cluster may use only a single port, dedicated per virtual CPU, on the load spreader to read the descriptors from the QoS Engine

10 Carrier Grade Quality of Service Engine

The QoS Engine is responsible for the queuing of PDUs stored in the shared buffer and the scheduling of PDUs for transmission on **egress** interfaces. It is also responsible for allocating egress bandwidth according to a configurable and controllable scheme (i.e. policy), allowing among other things, prioritization of traffic, fairness, and rate limit.

QoS Engine Features

- Supports 30M packets per second throughput
- Supports 256 queues
- Supports up to 90 egress ports
- Supports associating up to 8 queues per egress port
- Supports queue tail drop policies of types – fixed limit, RED and WRED
  - For queues with fixed limit drop policy, QoS has per queue thresholds (in units of packets and bytes) for green and yellow colored packets. After the threshold is crossed, packets of the specific color are dropped.
  - For queues with RED or WRED drop policy, RED/WRED is applied on each enqueued packet and the packet is either dropped or enqueued.
  - Supports color based RED/WRED parameters per QoS queue.
- Supports QoS scheduling for all egress ports
  - Supports a layered tree of scheduling policies starting with a set of queues and ending with a port. The flow is from the leaves (queues) through nodes and to the root (egress port).
  - Supports 8 layers of QoS node schedulers
  - Supports strict priority, and deficit weighted round robin per scheduling node
- Supports per node and per queue bit rate shaping
  - Supports group rate shaping where a group of nodes share a single rate shaper. The accuracy of rate shaper is better than 1%.
  - Supports 32 shared rate shapers, each assigned to 8 nodes or less
- Schedules packets based on application of all scheduling logic types together, i.e. apply both policing, individual rate shaping and group rate shaping.
- Allows changing scheduler (weights) and shaper parameters (information rates, burst sizes) while scheduler/shaper is active.

11 Coherent Processing Subsystem

Figure 11 depicts the Coherent Processing Subsystem (CPS) which consists of:

- 2 MIPS InterAptiv* cores
- 12 thread contexts
- 4 virtual CPUs
  - One watchdog timer (WDT) per virtual CPU
  - One interval timer per virtual CPU
- Coherence manager (CM)
- 2x IO coherence units (IOCU)
- L2 cache controller (L2$)
- Cluster power controller (CPC)
- Global interrupt controller (GIC)
- Inter-thread communication (ITC) unit
- Debug and trace system

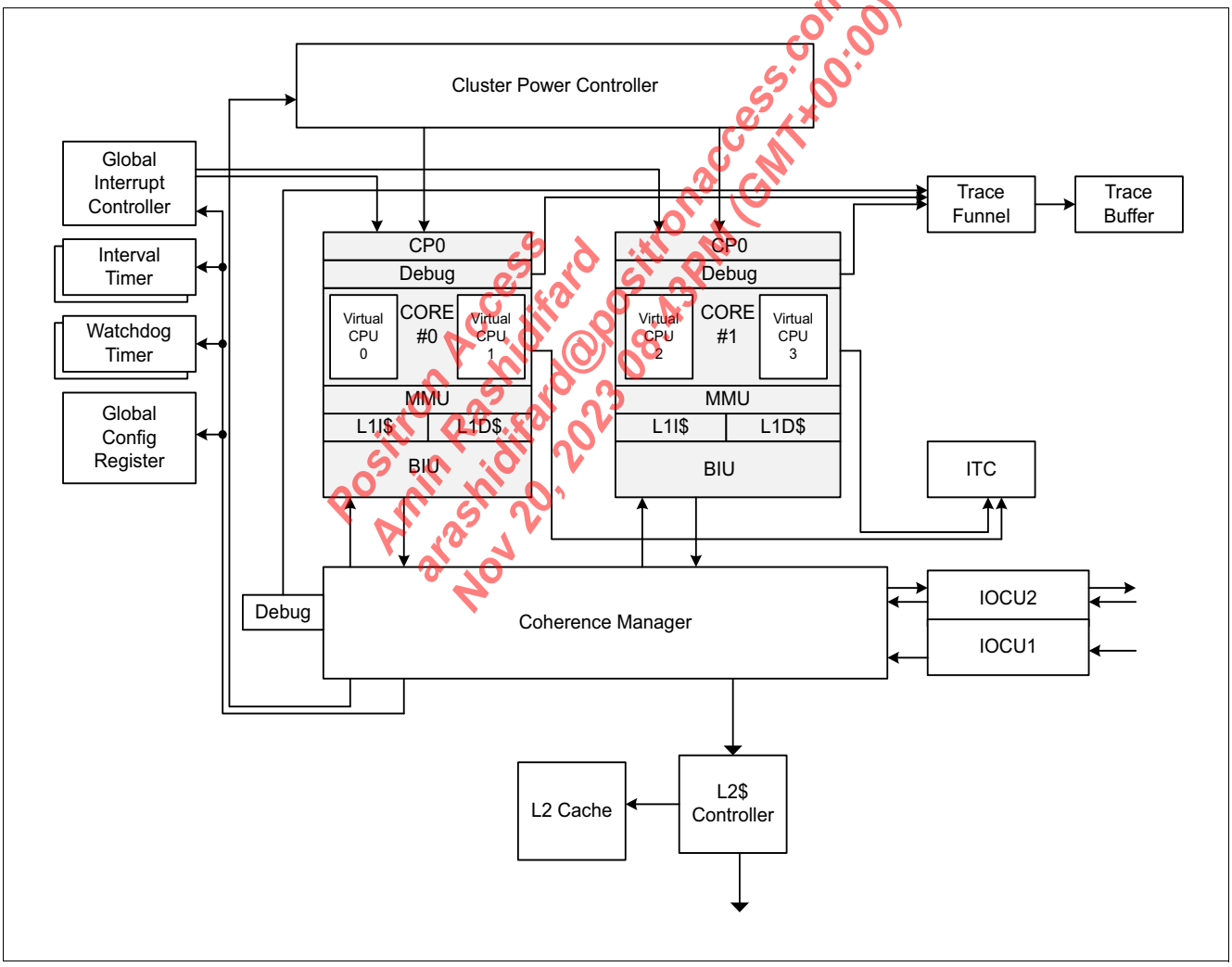


Figure 11 Overview of the Coherent Processing System

11.1 InterAptiv* Processor

The InterAptiv* processor provides these features:

- 9-stage pipeline
- 32-bit address paths
- 64-bit data paths to caches
- MIPS32* release 3 instruction set and privileged resource architecture
- MIPS MT ASE
  - 2 virtual CPUs per core which are also referred to as Virtual Processing Element (VPEs) [2]
  - 6 thread execution contexts (TCs) per core
  - Inter-thread communication (ITC) memory for efficient communication and data transfer
- MIPS DSP ASE
- Memory management unit
  - 32 dual-entry fully associative joint TLB (JTLB) per VPE
  - JTLBs are sharable under software control
  - Fully associative Instruction micro TLB (ITLB) with 3 shared entries and 1 private entry per TC
  - 8-entry fully associative data micro TLB (DTLB)
- L1 instruction cache (L1I$) and L1 data cache (L1D$)
  - 32 Kbyte instruction cache
  - 32 Kbyte data cache size
  - 4-way set associative
  - 8 outstanding data cache load misses
  - Supports write-back mode
  - 32 byte cache line size
  - Virtually indexed, physically tagged
  - Cache line locking support
  - Non-blocking pre-fetches
  - Hardware support of L1$ aliasing fix
- Core bus interface unit (core BIU)
  - OCP interface with 32-bit address and 64-bit data
  - OCP interface runs at CPU core clock
  - Burst size of four 64-bit beats
  - 4 x 32-Byte entry write buffer
- Multiply/divide Unit
  - Maximum issue rate of one 32 x 32 multiply per clock
  - 5 cycle multiply latency
  - Early-in iterative divide. Minimum 11 and maximum 34 clock latency (dividend (rs) sign extension-dependent)
- Clock gating based power control
  - Minimum frequency: 0 MHz
  - Power-down (clock gated) mode triggered by WAIT instruction
  - Support for software-controlled clock divider: dividers are inside chip CGU, different clock frequency is used to supply to CPU
  - Extensive use of local clock gating

11.1.1 Virtual CPU

Two virtual CPUs are implemented per core, referred as Virtual Processing Element (VPE) in the MIPS document [2].

11.1.2 Thread Context

Six thread contexts (TC0-TC5) are implemented per core.

11.1.3 Execution Unit

The core execution unit implements a load-store architecture with single-cycle arithmetic logic unit (ALU) operations (logical, shift, add, subtract) and an autonomous multiply-divide unit. Each TC on the core contains thirty-two 32-bit General-Purpose Registers (GPRs) used for scalar integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

11.1.4 Multiply/Divide Unit

The Multiply/Divide Unit (MDU) performs multiply and divide operations. The MDU consists of a pipelined 32x32 multiplier, result-accumulation registers (HI and LO), multiply and divide state machines, and all multiplexers and control logic required to perform these functions. This pipelined MDU supports execution of a multiply or multiply-accumulate operation every clock cycle.

11.1.5 System Control Co-processor CP0

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, cache protocols, the exception control system, the processor diagnostics capability, operating mode selection (kernel vs. user mode), and the enabling/disabling of interrupts. Configuration information such as cache size, set associativity, and presence of build-time options is available by accessing the CP0 registers.

11.1.5.1 Watch Register

The watch register is used to store an exception address for either instruction fetch or data access. When the watch register content matches the actual access, the watch exception happens. This facilitates software debugging.

11.1.5.2 Processor Identification and Virtual CPU Number

The CPU number in a multi-processor system is specified in register VPEx_CP0_EBase. CPUNum is used by software to distinguish a particular CPU core from the others.

Table 27 shows the coding of VPEx_CP0_EBase.CPUNum.

Table 27 CPU Number

Processor		Register	Description
CORE0	VCPU0	VPE0_CP0_EBase.CPUNum	$00\ 0000\ 0000_B$
	VCPU1	VPE1_CP0_EBase.CPUNum	$00\ 0000\ 0001_B$
CORE1	VCPU2	VPE0_CP0_EBase.CPUNum	$00\ 0000\ 0010_B$
	VCPU3	VPE1_CP0_EBase.CPUNum	$00\ 0000\ 0011_B$

11.1.5.3 Endianness

A CPU core is operated either in big endian or little endian mode. The endianness is selected by boot strapping.

The status of the endianness selection signal is read in VPEx_CP0_Config.BE.

11.1.5.4 CPU Performance Counter

Each TC has two 32-bit performance counters and each core has 12 performance counters altogether.

The performance counter registers are connected to a clock that is stopped when the processor is in sleep mode. This must be considered when analyzing measurements taken on the system.

11.1.6 Memory Management Unit

This description holds for each VPE of both cores, VPEx = VPE0 and VPE1. The CPU core contains a memory management unit (MMU) per VPE that interfaces between the execution unit and the cache controllers.

Each MMU is based on a translation lookaside buffer (TLB). The TLB consists of three translation buffers when JTLBs are shared or four translation buffers when JTLBs are independent.

- 32 dual-entry fully associative joint TLB (JTLB) per VPE
- Fully associative instruction micro TLB (ITLB) with 3 shared entries and 1 private entry per TC
- 8-entry fully associative data micro TLB (DTLB)

The ITLB and DTLB, also referred to as the micro TLBs, are managed by the hardware and are not software visible. The micro TLBs contain subsets of the JTLB. When translating addresses, the corresponding micro TLB (I or D) is accessed first. When there is no matching entry, the JTLB is used to translate the address and refill the micro TLB. When the entry is not found in the JTLB, an exception is taken.

11.1.7 Exception Handling

This section describes these exceptions in detail, which are caused external to the CPU core. They are described in the relative priority, highest to lowest. The CPU core provides several exceptions, which are generated internal to the CPU core, e.g. arithmetic overflow. These exceptions are not covered in detail in this section, see the appropriate MIPS documentation.

Table 28 summarizes all exceptions.

Table 28 Priority of Exceptions

Exception	Description
Reset	Reset Exception
DINT	Debug Interrupt Exception
NMI	Non Maskable Interrupt Exception
Interrupt	Interrupt Exception
IBE	Instruction Fetch Bus Error Exception

11.2 Coherence Manager Overview

The coherence manager (CM) is responsible for establishing the global ordering of requests as well as collecting the intervention responses and sending the correct data back to the requester. **Figure 12** shows a high-level view of the coherence manager.

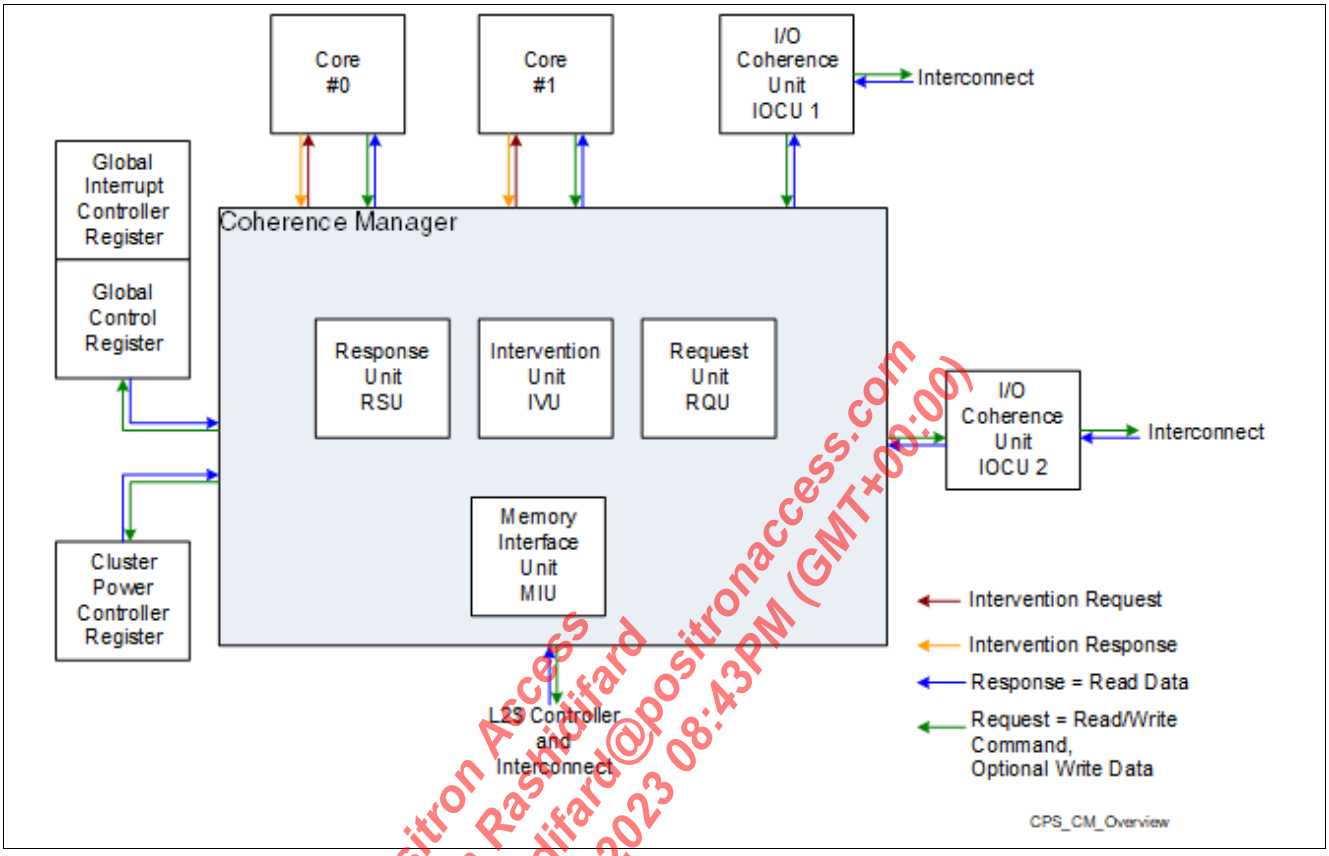


Figure 12 Coherence Manager Overview

Request Unit

The Request Unit (RQU) receives requests from the coherent CPU cores as well as the IO Coherence Unit (IOCU, also called agents) and serializes them. Non-coherent requests are forwarded either to the Memory Interface Unit (MIU), to the IOCU or to the memory-mapped register accesses to the GCR, GIC and CPC. Coherent requests are sent to the Intervention Unit (IVU).

Intervention Unit

This block receives the serialized stream of coherent requests from the request unit. These requests are sent as interventions to all the coherent devices, which update their cache states appropriately for the intervention and provide a response. When a requested cache line is in an exclusive or modified state, the data is returned with its response on a read type intervention. The Intervention Unit gathers the responses from each of the agents and takes care of these actions:

- Speculative reads are resolved (confirmed or canceled)
- Memory reads that are required because they were not speculative are issued to the memory interface unit
- Any modified data returned from a coherent device is sent to the memory interface unit to be written back to memory
- Any data returned from a coherent device is forwarded to the Response Unit to be sent to the requester
- The MESI state in which the line is installed by the requesting CPU is determined (the install state). When there is no other CPU with the data, a shared request is upgraded to exclusive

Memory Interface Unit

The MIU handles the interface to the L2/memory. Non-coherent reads and writes as well as speculative coherent reads are sent to the memory interface unit from the request unit. Coherent writes and late reads are generated from the intervention unit.

This block is responsible for staging the read data back to each of the agents. There are independent staging registers for each agent, which allows concurrent data return to different agents. This block stores the read data returned from the system when the read is still speculative or when the response unit is busy.

Response Unit

This block is responsible for returning data to the requesting agent. It sends data from the intervention unit, the memory interface unit, the IOCU, or from memory-mapped register accesses to the GCR, GIC and CPC.

11.3 L2 Cache Overview

The L2 cache controller (L2$) has two Open Core Protocol (OCP) interfaces. On the OCP slave interface OCP-S, it communicates with the Coherence Manager (CM), and on the OCP master interface OCP-M, it communicates with the interconnect. The L2 cache controller also communicates with the processor through the performance counter interface, error reporting interface, and other side band signals.

11.3.1 L2 Cache Attributes

Table 29 shows the L2 cache attributes.

Table 29 L2 Cache Attributes

Attribute	Value	Description
Size	256 Kbyte	The size of the L2 Cache is 256 Kbyte.
Size	128 KByte	The size of the L2$ is 128 KByte
Size	128 KByte	The size of the L2$ is 128 KByte
Line Size	32 byte	The L2 Cache line size is 32 byte.
Associativity	8 way 4 Way	The L2 Cache is 8 way 4 waysassociative.
Parity	No	No parity protection for the L2$ arrays is implemented.

11.3.2 L2 Cache Protocols

The L2 cache controller supports these cache protocols.

Uncached

Addresses in a memory area indicated as uncached are not read from the L2$. Stores to such addresses are written directly to main memory, without changing L2$ contents.

Write-through, no write-allocate

Read requests first search the L2$, reading main memory only when the desired data does not reside in the L2$. On data store operations, the L2$ is first searched to see when the target address is cache resident. When it is resident, the cache contents are updated, and main memory is also written. When the cache look-up misses, only main memory is written.

Write-back, no write-allocate

Read requests are handled the same as write-through. Stores that hit in the cache only update the cache contents but are not written to main memory. Stores that miss in the cache do not cause a cache refill and the data is written directly to main memory.

Uncached Accelerated

Treated like uncached access. No additional write merging is performed by the L2 controller. When an uncached accelerated write was originated as a burst on the slave interface, the burst is maintained on the master interface.

Write-back, write-allocate

Read requests and write requests that hit in the L2 cache are handled the same as write-back, no write-allocate. When the write requests miss in the cache and the requests are full cache line writes, the data is written to the cache. It does not cause a cache refill because only full cache line writes are allocated. However, it causes an eviction to create room for the write data.

Allocate on read miss/No allocate on read miss

When the read requests miss in the cache, the main memory is read and the cache is updated with the data being returned. However, L2 cache also supports a mode that the return data is passed to the core without allocating into L2 cache.

11.4 IO Coherence Unit

The IO coherence unit (IOCU2) consists of two channels, the IO Initiator request/response channel (IO) and the memory mapped request/response channel (MMIO), the IOCU 1 has one IO Initiator request/response channel.

IO Initiator Request/Response Channel

The IO initiator request/response channel (IO) within the IOCU is responsible for translating non-coherent read/write transactions to the appropriate coherent or non-coherent transactions. Finally, these translated transactions are issued to the CM. The non-coherent read/write transactions are initiated by system masters, e.g. DMA controller, which are located at the non-coherent interconnect.

The CM routes non-coherent transactions directly to the L2$. Coherent transactions are snooped in the L1D$ of all CPUs via their intervention ports. In the case of an L1D$ hit, read data is returned directly via the IOCU to the system master. Write data is merged and written to the L2$ or main memory.

Memory Mapped Request/Response Channel

The MMIO within the IOCU is responsible for forwarding read/write transactions initiated by the CPUs to the non-coherent interconnect (SSX7). Corresponding response data is routed from the non-coherent system back to the CM.

12 Boot/TEP Secure Boot Core

Secure Boot core is also called trusted execution processor (TEP).

This chapter describes the dedicated MIPS 4KEc* core and its subsystem. The core is used as:

- Boot Core in standard boot products
- Secure Boot core in Secure Boot products

12.1 MIPS 4KEc* Features

The MIPS 4KEc* core supports:

- 32-bit address paths
- 32-bit data paths
- MIPS32* compatible instruction set
  - All MIPS II* instructions
  - Multiply-add and multiply-subtract instructions (MADD, MADDU, MSUB, MSUBU)
  - Targeted multiply instruction (MUL)
  - Zero and one detect instructions (CLZ, CLO)
  - Wait instruction (WAIT)
  - Conditional move instructions (MOVZ, MOVN)
  - Prefetch instructions (PREF)
- MIPS32* enhanced architecture (Release 2) features
  - Vector interrupts and support for external interrupt controller
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - Bit field manipulation instructions
- MIPS16e* application specific extension
  - 16 bit encoding of 32 bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - Data type conversion instructions (ZEB, SEB, ZEH, SEH)
  - Compact jumps (JRC, JALRC)
  - Stack frame set-up and tear down macro instructions (SAVE and RESTORE)
- Instruction and data cache
  - 32 Kbyte instruction cache size in a 4-way set associative organization
  - 32 Kbyte data cache size in a 4-way set associative organization
  - Loads blocks only until critical word is available
  - Supports write-back with write-allocation and write-through with or without write-allocation
  - 16-byte cache line size, word sectored
  - Virtually indexed, physically tagged
  - Support for cache line locking
  - Non-blocking prefetches
- MIPS32* privileged resource architecture
  - Count/compare registers for real-time timer interrupts
  - Instruction and data watch registers for software breakpoints
  - Separate interrupt exception vector
- Memory management unit
  - 32 dual entry JTLB with variable page size
  - 4-entry instruction micro TLB
  - 4-entry data micro TLB

- Core nus interface unit (Core BIU)
  - All I/Os fully registered
  - Two 16 bytes collapsing write buffers
- Multiply divide unit
  - Maximum issue rate of one 32 X 16 multiply per clock
  - Maximum issue rate of one 32 X 32 multiply every other clock
  - Early-in divide control. Minimum 11, maximum 34 clock cycles
- Big and little endian support
- Access to NGI as trusted initiator
- Power control
  - No minimum clock frequency
  - Power down mode (triggered by WAIT instruction)

12.2 Secure Boot Core UART

The UART has 16-byte FIFOs on its RX and TX paths. It is possible to configure its parity mode and number of stop bits.

The UART is able to generate several IRQs – RX/TX FIFO levels, parity error, Rx idle condition (a case where the RX watermark level was not reached after some idle time, but the UART RX FIFO still has some information inside).

13 Trusted Execution Environment

This chapter describes the trusted execution environment (TEE) from the hardware design perspective, including the secure boot core which is targeted to run the secure OS and software.

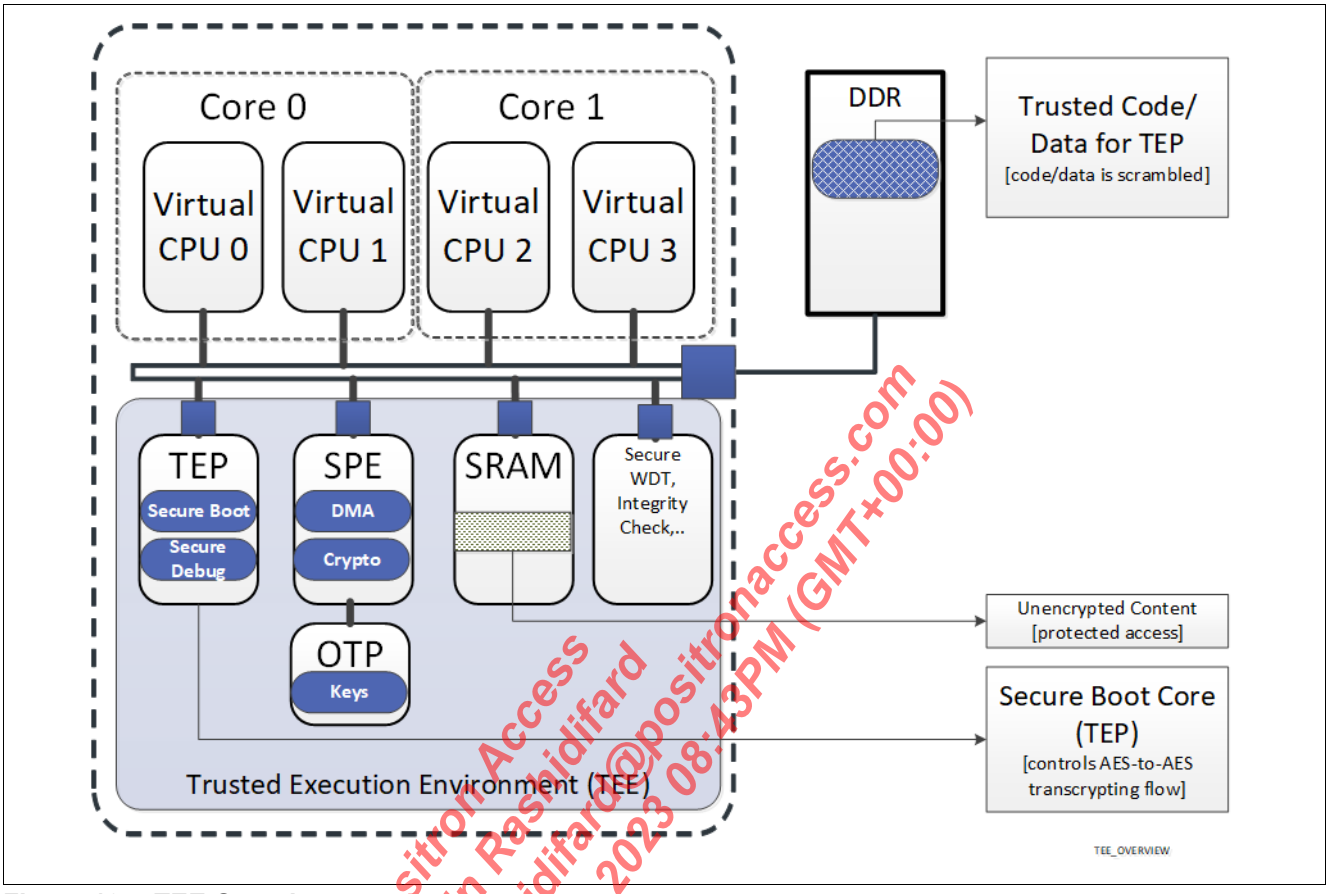


Figure 13 TEE Overview

13.1 Features

The TEE provides these features:

- Dedicated MIPS 4KEc* core as secure boot core (TEP)
- Security and firewall functionality in each target agent via protect region
- Setup of access permissions of protected regions only through TEP
- Configuration of the chip GPIO interface functionality only through TEP
- Trusted storage achieved with trusted access to secure platform engine (SPE) and trusted application execution

13.2 TEP Access to Platform Resource

This section describes the TEP access rights.

13.2.1 Root of Trust

The root of trust is stored inside the OTP. The access to OTP is limited to trusted platform engine, while only TEP is allowed access to this engine via mailbox exchange.

13.2.2 Access Protection

The access protection to other on chip/off chip resources is achieved via access initiator to address region mapping.

Each access initiator is assigned with dedicated initiator ID; based on this ID, the interconnect allows/stops access to certain address region. The ID to region mapping is defined in interconnect register, and these registers are only allowed to be set up or changed by the TEP. See **Interconnect Protection Mechanism** for details.

For chip interface multiplex control register, only TEP is assigned the access rights.

13.2.3 InterAptiv* CPU Cluster Initial ID Adaptation

In a cluster CPU subsystem, the CPU tag signal behaves differently for cached L2 and uncached L2 (L1 is cached) to interconnect.

- Cached access, after L2$, the CPU tag is lost;
- Uncached access, CPU/VPE/TC tag is maintained.

As such, an ID adaptation is required for uncached access to identify which access is from which TC. For cached access, a default ID of 0 is generated.

Table 30 Initiator ID Adaptation (Hardware Default)

Access Source	CPU0, VPE0	CPU0, VPE1	CPU1, VPE0, all TCs	CPU1, VPE1, all TCs
Cached Access, Resulted MConn_ID	0	0	0	0
Uncached access, Resulted MConn_ID	0	0	0	0

Table 31 Initiator ID Adaptation (Reprogrammable via GCR Registers)

Access Source	CPU0, VPE0, TC0	CPU0, VPE0, not TC0; VPE1, all TCs	CPU1, VPE0, all TCs	CPU1, VPE1, all TCs
Cached Access, Resulted MConn_ID	0	0	0	0
Uncached access, Resulted MConn_ID	2	1	0	4

Attention: It is only possible to program the Initiator IDs 0, 1, 2, 4.

13.3 Interconnect Protection Mechanism

This section describes the interconnect protection mechanism.

13.3.1 Identification

The initiator identification InitID is used for debug purposes at each target agent (TA) to identify the initiator of the transaction, the system master(s) connected to an initiator agent (IA).

There is a unique master identification MasterID assigned to each system master. This MasterID is global for all Instances and is mapped onto the IA_MConnID signal. Thus, the MasterID travels along with the transaction from the initiator (system master) to the target (system slave).

13.3.2 Protection Overview

The NGI allows access to specified target agents (TA) to be restricted, protecting these TAs and their connect system slaves from unauthorized access. The protection mechanism is based on the use of flexible, pre-programmed protection regions that enable fine-grained access control at the TA based on these attributes of each request.

- Address
  The value of MAddr is used to determine the protection region. Because the IA is able to do address fill-in and/or multi-channel operations based on the initiator's MAddr signal, the address received by a TA may not be the same as the address sent by the initiator.
- Initiator ID InitID
  Used to determine the initiator read or write permissions within the protection region.
- MCmd
  Used to determine when a read or write is requested.
  The ReadEx command is evaluated as both a read and a write.

13.3.3 Interaction with Software

Setting up the protection region register needs to be performed only by TEP. This is done by setting up the XBAR registers into two portions.

- Part 1 registers, which starts with tREG_PM_*, are only programmed by TEP.
- Part 2 registers are accessible by all CPUs.

13.4 Secure Platform Engine

The secure platform engine is to protect embedded systems against hackers trying to install hacked OS, copy hacked software image to other system, and protect device manufacturer's software against illegal copying.

The SPE together with the **OTP Memory** supports secure boot/platform with these key elements:

- On-chip OTP module to store the root of trust assets
- Cipher algorithm: AES in CBC mode with 256 bit key
- Hashing: SHA2 with 256 bit key
- True Random Number Generator (TRNG): hardware-based TRNG for IVs, nonces, public and private keys
- Secure debug
- Crypto algorithm specific block data de-/encryption (host must pad/remove padding for non-block size data) AES: multiples of 16 bytes

13.4.1 OTP Memory

16 Kbits OTP memory is used as the Non-Volatile Memory (NVM). The NVM layout and structure are described in this section.

NVM Access Mapping by Secure Boot Engine

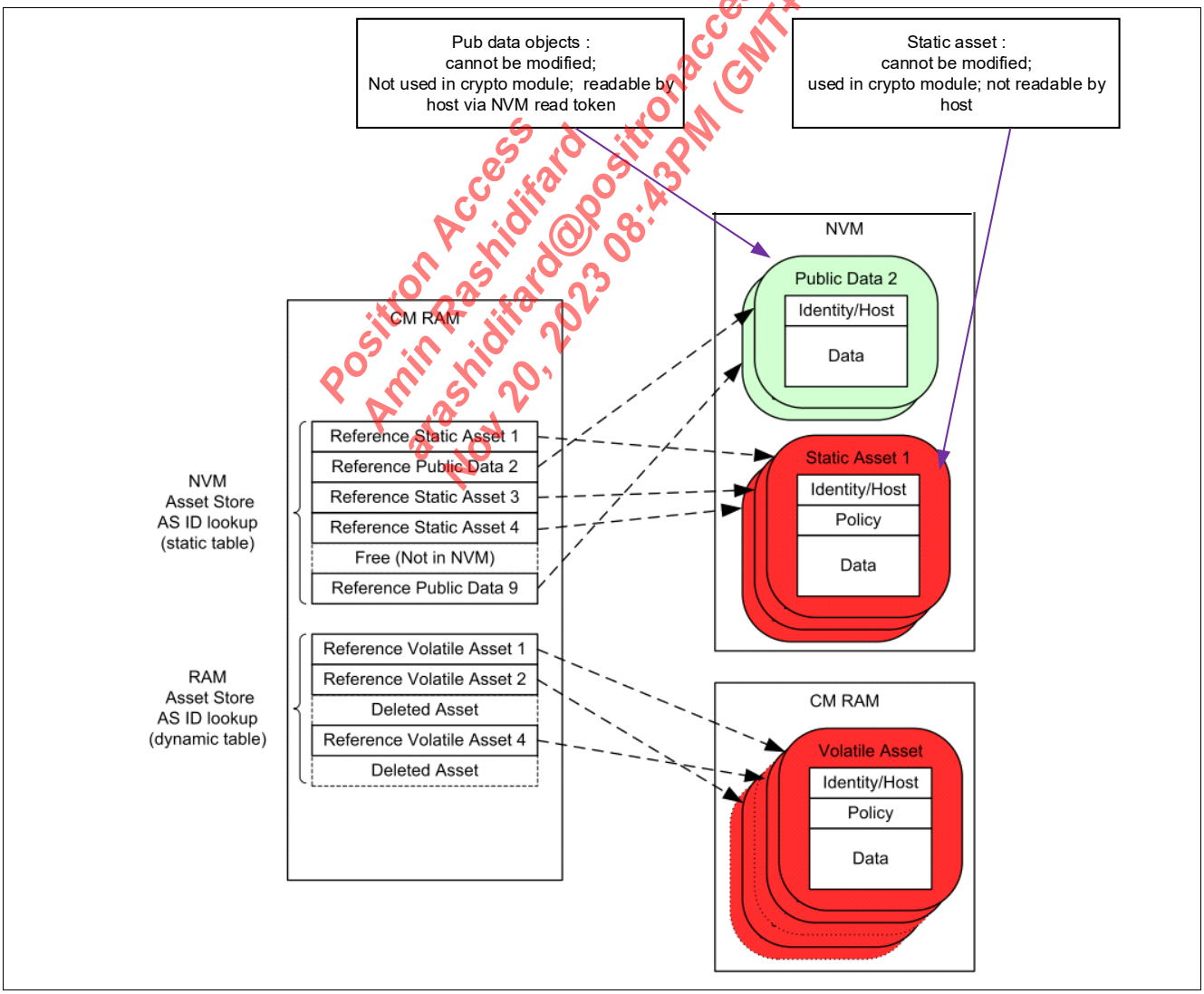


Figure 14 NVM Mapping

It is possible to have up to 62 assets inside the NVM. Each asset is indexed according to the header ID of the data objects. The asset is deemed deleted when the header ID is all programmed, e.g. 0x3F, the secure boot engine no longer indexes the deleted asserts or reads them out.

A protected asset is not allowed to be deleted and such operation is rejected.

OTP Data Example

Figure 15 gives an example of OTP data layout. Access to the secure data (encryption keys, key hashing, etc.) is strictly limited to the Secure Boot engine only.

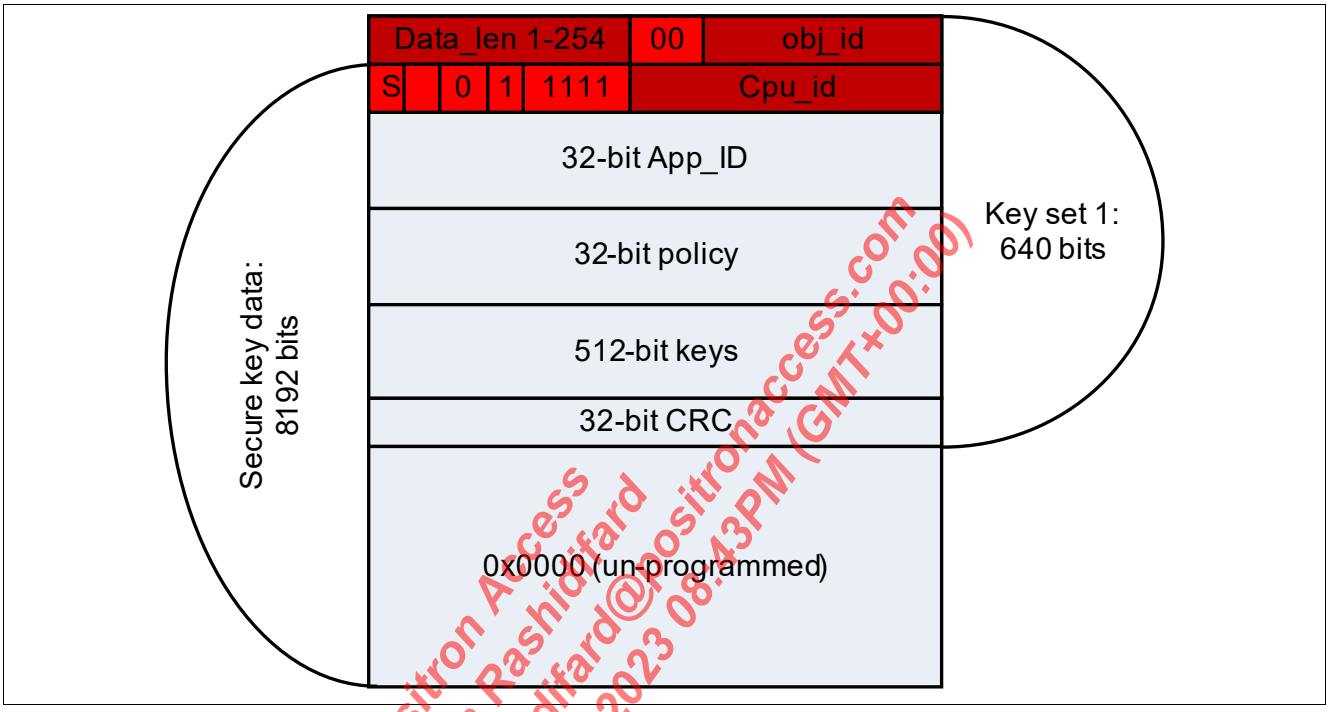


Figure 15 OTP Data Example

Secure Boot Package

MaxLinear provides secure boot package documents that describe how to create NVM data image and program NVM, how to create secure boot application images. The documentation is available on request.

14 Boot System

This chapter describes the features of the boot system.

14.1 Features

The boot system offers the following features.

- Booting from QSPI interface (multiplexing on GPIO0, 1, 2, 3, 4, and 5) with internal ROM
  - 1 bit mode of QSPI NOR, QSPI NAND
  - 4 bit mode of QSPI NOR, QSPI NAND
- Boot from internal ROM using legacy UART#0 RS232 (ASC) and UART#0 XMODEM.
- Multiple (up to 4) duplicated images for booting system reliably
- DDR sub-system configuration and tuning
  - Register programming via encapsulated command from flash
  - White-list register access to prevent wrongly writing into unintended register
- Secure Boot
  - Root of trust secure boot for production provision
  - TrustWorld secure boot for secure boot enabled end products
- Boot from NAND with internal ROM using QSPI supporting:
  - Refer to the reference board design guide [8] for supported NAND flash types
  - Boot from 512 Mbit, 1 Gbit, 2 Gbit,4 Gbit, and 8 Gbit size NAND flash
  - Boot from NAND flash with hardware ECC embedded inside flash device
  - QSPI NAND bad block management with ONFI or fixed size via different pin strap options

14.2 Functional Description

This section describes the hardware conditions after power-on-reset (POR) and describes the boot loader for on-chip ROM implementation. This boot loader stores codes in hardware mainly to:

1. Pre-configure the system, and
2. Handle the (boot) code download from an external non-volatile memory through a target peripheral interface.

14.2.1 Boot Selection after POR

The hardware status after POR is as follows:

- All MIPS hardware module interrupts are disabled.
- A reset status register in RCU stores the on-board pin strapping information.

The boot selection process is completely done by hardware, no ROM code involvement yet.

Table 32 Boot Mode Settings

Strap Select					1st Boot Source	2nd Boot Source
BOOT 3 (UTXD0)	BOOT 2 (GPIO31)	BOOT 1 (GPIO16)	BOOT 0 (GPIO1 and GPIO0)	HEX		
0	0	1	0	0x02	**ROM**	**UART0 XMODEM** This mode boot from UART0 with XMODEM protocol.
0	1	0	0	0x04	**ROM**	**Legacy UART0** This mode boot from UART0 using legacy mode.
0	1	1	1	0x07	**ROM**	**QSPI (Single Bit NAND), Bad Block management enabled, fixed block size**
1	0	0	0	0x08	**ROM**	**QSPI (Single Bit NOR)**
1	0	0	1	0x09	**ROM**	**QSPI (Single Bit NAND), Bad Block management enabled, ONFI mode**
1	0	1	0	0x0A	**ROM**	**QSPI (Quad Bit NAND), Bad Block management enabled, fixed block size**
1	0	1	1	0x0B	**ROM**	**QSPI (Quad Bit NOR)**
1	1	0	0	0x0C	**ROM**	**QSPI (Quad Bit NAND)**
1	1	0	1	0x0D	**ROM**	**QSPI (Single Bit NAND)**
1	1	1	0	0x0E	**ROM**	**QSPI (Quad Bit NAND), Bad Block management enabled, ONFI mode**
				Others	**Reserved**	

15 Multi-core Processing Engine

The multi-core processing engine (MPE) uses processor resources of the CPS cluster in form of a configurable number of virtual CPUs and thread contexts (TCs).

The complete multi-core processing engine solution includes MPE control, search, metering, and copy engines.

The buffer manager and carrier grade quality of service engine are the key elements in providing the connectivity between the subsystems as well as guaranteeing the required flow priorities.

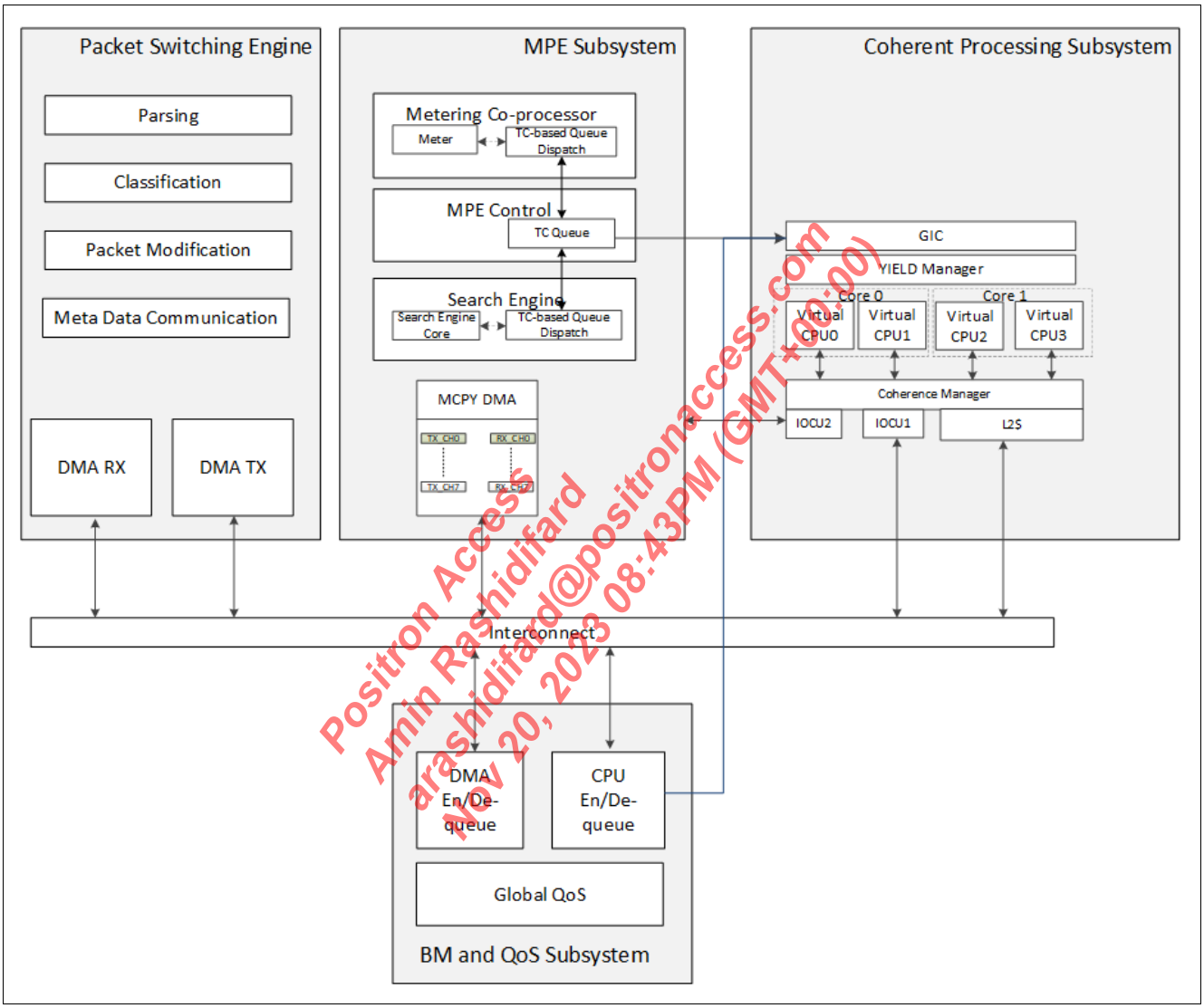


Figure 16 Multi-core Processing Engine

15.1 MPE Features

The MPE features are:

- Firmware-based packet processing
- Firmware interacts with the BM and QoS engine through interrupts/yields and register reads/writes and is not involved in data path handling
- Header based packet processing architecture. No payload copies into processor cache
- In-band meta data communication protocol with packet switching engine
- Post processing header construction offload by dedicated cache coherent memory copy (MCPY) DMA
- Cache coherent search engine
- Meter co-processors
- True multithreading operation with parallel PDU processing context handling that ensure maximum utilization of virtual CPUs and TCs

15.2 Hardware Modules

The search engine and the meter engine are the two co-processors used by the MPE firmware.

The MPE firmware interacts with the hardware engines using the command and response registers and the queues in the MPE Controller.

The MPE firmware also interacts with the MemCopy (MCPY) hardware engine to initially load the packet header into the L2 cache and for header copy to the external memory after the header modification is complete.

15.2.1 Search Engine

The MPE firmware sets up the search command for search operation and issues the search command to the search engine HW using the respective TC command register. These are the modes in which the search engine performs the search operation:

- Manual mode
- Auto mode

In the manual mode, the MPE firmware must create a search command block which has the information on the key, mask and the key size. In the search command, the firmware passes the address for this SCB to the search engine. The search engine hardware reads this block and performs the search operation.

In the auto mode, the MPE firmware provides the base address of the packet header it received from the CQE. It also provides a field mask in the command. On receiving the search command, the search engine needs to load the parser and header information from the memory and create the search key with the predefined fields from the header. After the creation of the key and the mask, the search engine hardware performs the search operation.

The MPE search engine compare tables are maintained in the DDR memory. The search engine hardware supports up to 8 compare tables. The table to be used for the particular search operation is chosen by the firmware in the search command.

15.2.1.1 Search Engine Features

The search engine supports these features:

- Option for automatic key formation by hardware or flexible firmware defined key
- Up to 8 compare tables
- Configuration to choose between linear and hash based tables
- Search is only triggered by MPE command
- 64k sessions (hash-based)

15.2.2 Metering

The metering supports these features:

- Total 16 double rate three color metering instances
- Up to two cascaded metering instances are assigned to measure the rate of a packet
- Metering is triggered by either the MPE command or by the two parallel CPU control registers

15.2.3 MPE Controller

The MPE controller maintains queues through which the MPE hardware and MPE firmware interacts. The MPE firmware (TCs) issues commands to the MPE hardware through the command registers and reads the response from the response registers. There are separate command and response registers for each TC. The MPE controller also provides a mechanism for inter-TC communication which the TCs use to pass on information to each other during processing.

The MPE controller has these queues:

- One free queue for enqueue of commands
- 12 TC queues for communicating with the TCs
- One search engine queue to interface with the search engine hardware
- One metering engine queue to interface with the metering engine hardware

15.2.4 Coherent Memory Copy Engine

The coherent memory copy engine (MCPY) performs a copy operation without additional system involvement.

The system software simply provides the source address, destination address and amount of data to be copied.

These features are supported.

- Handling of unaligned memory access; there is no requirement for data to be on DWORD boundaries.
  – This way there is no need for word boundary checks in the memory copy routine.
- Total 8 request ports available to accept memory copy request commands.
- MCPY is able to process multiple small chunks of data – the transfer of one large block of data does not block all other requests until it is finished.
- Data gathering mode: MCPY is able to gather fragments of a large block of data in non-continuous memory locations into a single block at one continuous memory location.
- The source and the destination address must be physical address.

16 DDR SDRAM Controller

The DRAM controller manages the off-chip DRAM and provides a mechanism for other functional units to access the DRAM. The memory controller supports a total memory size of 64 MB to 1 GB, via a DDR3(L)/DDR4/LPDDR3 channel with 16-bit or 32-bit data bus width.

16.1 DDR SDRAM System Overview

Figure 17 illustrates the DDR SDRAM system which consists of:

- A DDR universal protocol controller
- A DDR SDRAM PHY utility block
- A DDR SDRAM PHY (including PADs)
- DDR SDRAM devices

These DDR speed grades are supported.

- DDR3(L)-1066, DDR3(L)-1333, DDR3(L)-1600, DDR3(L)-1866, and DDR3(L)-2133
- DDR4-1866 and DDR4-2133
- LPDDR3-1066, LPDDR3-1333, LPDDR3-1600, LPDDR3-1866, and LPDDR3-2133

All memory devices must be soldered on the main board. There is no support for DIMMS.

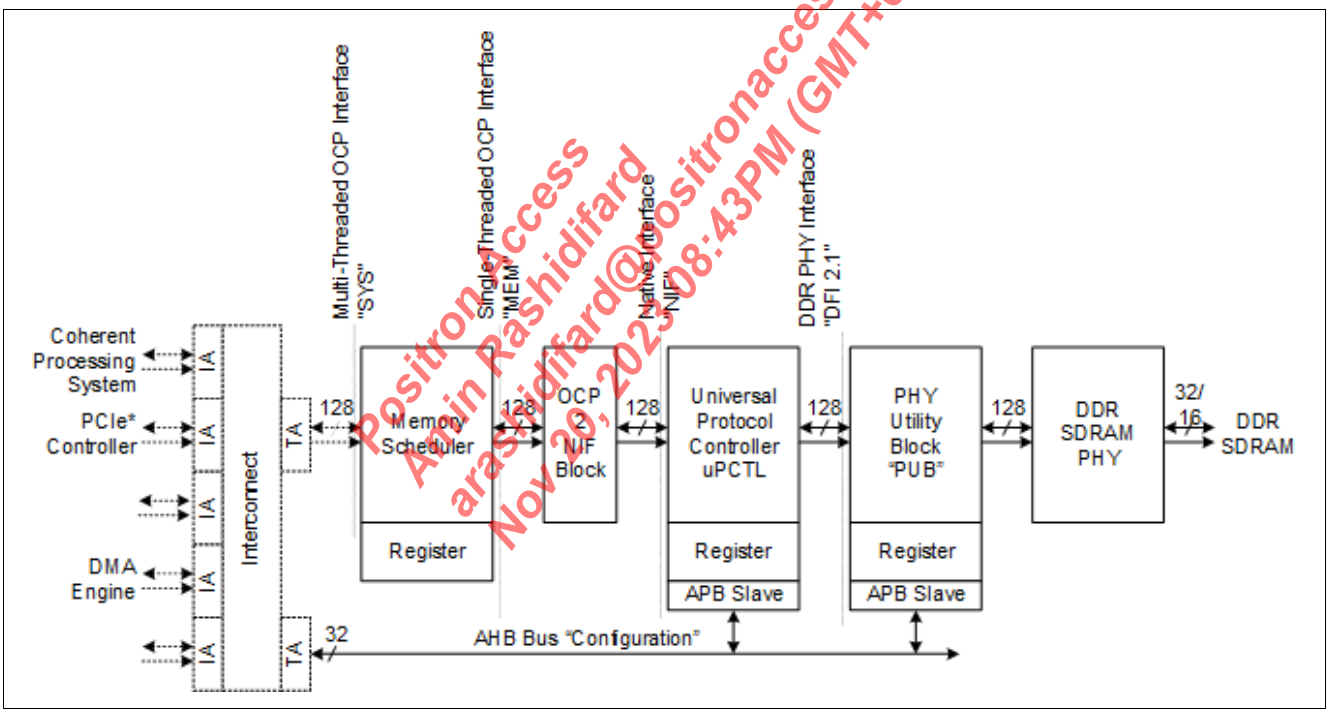


Figure 17 DDR SDRAM System Block Diagram

16.2 Memory Access Scheduler

The memory access scheduler is responsible for converting the system internal access into DRAM commands and scheduling optimized access command sequence.

16.2.1 Features

The memory access scheduler provides these features:

- Quality-of-Service (QoS)
  - Per-thread QoS scheme selection priority, allocated bandwidth and best effort
  - Higher priority thread requests achieve extremely low latency
  - Guaranteed BW threads to minimize buffering/receive latency
  - Per-tag starvation avoidance
  - Keeps DDR page open as long as possible
  - Groups reads and writes towards DDR to achieve maximum utilization
  - Minimizes DDR Rank crossing
- Reorder of requests on different threads and tags to maximize efficiency
- User-configurable address tiling function
  - Transforms request addresses
  - Improves DDR SDRAM bandwidth efficiency

16.2.2 QoS Arbitration and Levels

Supported arbitration and levels are described in this section.

16.2.2.1 Per Tag Arbitration

A thread is assigned with a weight, a counter counts down from the weight, each transfer scheduled counts once, when the counter reaches 0, it then wraps around to the initial weight value again.

16.2.2.2 Per Thread Arbitration

A thread is assigned with different QoS level (priority, bandwidth, and best-efforts), the QoS algorithm ensures priority threads minimize the latency while within bandwidth allocation, bandwidth threads get guaranteed bandwidth.

16.2.2.3 QoS Levels

Three levels of QoS are supported:

- Best-effort
- Allocated bandwidth (minimum sustainable bandwidth such as video)
- Priority (minimum latency such as cache refill)

16.2.2.4 Dynamic QoS Level Adjustment

The adjustment is made based on a per-thread credit value that indicates when a thread is being over or under serviced. The value of 0 means the thread is brought serviced correctly and stays at its programmed QoS level, a positive value means it is under serviced, it is promoted to the programmed QoS level. Higher QoS level threads always win the arbitration. A serviced thread credit is reduced. When its credit becomes negative, then this thread is being over served and it is demoted to best effort QoS level. The credit value by default increases at a rate consistent with the user specific bandwidth allocation.

16.3 DDR Universal Protocol Controller

This section introduces the Universal Protocol Controller (uPCTL).

16.3.1 Features

The controller supports these features:

- x16 or x32 memories for a 32-bit memory data path
- x8 or x16 memories for a 16-bit memory data path using DQ[15:0]
- Byte lane swapping is not supported for LPDDR3 devices
- Byte lane swapping is supported for the DDR4/DDR3(L) devices in which the operations are independent of DQ ordering
- Two memory ranks, devices within a rank tie to a common chip select
- Up to 8 memory banks
- Efficient DDR protocol with in-order column commands and out-of-order activate and precharge commands
- Down to 5 clock cycles command latency
- Automatic power-down and self-refresh entry and exit, driven from software and hardware
- Programmable per rank memory ODT
- Programmable data training assists in training of the data eye of the memory channel
- Programmable page policy
- Optimizes intelligent precharge/activate timings
- Reads reorder buffer to hold the data corresponding to a DDR command
- DDR controller Core clock at half of the DDR interface clock (1:2 clock ratio)
- DDR4 features
  - DBI (data bus inversion)
  - MPR reads and writes
  - Command/address parity error
  - Per DRAM addressability (PDA), e.g. program ODT or Vref on a DRAM device of a given rank
  - Programmable address latency
  - CRC on data bus for write access (DRAM device compares the CRC checksum coming from the controller, it flags CRC error when there is a mismatch)

16.3.2 Data Eye Training Control

The internal data test unit module generates data patterns to assist in bit de-skew, data eye training and long term bit error rate (BER) characterization. The data patterns are written into memory then read back to automatically adjust the DQS timing. To minimize the BER, random patterns are continuously written and read back to check external memory bank robustness against VT (voltage, temperature) change.

16.4 DDR PHY Utility Block

The PHY utility block (PUB) is used to connect the DDR controller and DDR PHY, it is JEDEC standard based. The PHY PUB supports the DDR3/DDR3L (JESD79-3F/79-3-1) **[25]**, DDR4 (JESD79-4) **[26]**, and LPDDR3 (JESD209-3C) **[27]** modes.

16.5 DDR SDRAM PHY

The DDR PHY handles the physical layer protocol including timing, signaling, and electrical aspects. The PHY complies with JEDEC standard.

- Embedded PLL and DDLs for meeting timing specification
- Write leveling delay lines to compensate address and control versus data delays
- Write and read bit delay lines to compensate per-bit delay skew
- Spread spectrum clock support

16.6 SSTL IO Block

The SSTL I/O are interface to the DDR device. The features are described here.

16.6.1 Features

These features are supported:

- Programmable input termination
  - DDR3(L): 40, 60, and 120 Ω
  - LPDDR3: 120 and 240 Ω
  - DDR4: 34, 40, 48, 60, 80, 120, and 240 Ω
- Programmable output impedance
- PVT compensated ODT
- Receiver power down control
- Power on Clear feature to be power supply sequence agnostic

16.6.2 ZQ Calibration Cell

The calibration provides capability for pull-up and pull-down input impedance as well as output impedances of the SSTL I/O. An external 240 Ω +/-1% resistor must be connected from the ZQ pin to ground.

16.7 DDR SDRAM Device Support

The DDR SDRAM controller supports:

- DDR3(L) and DDR4 SDRAM devices (Table 33), and
- LPDDR3 devices (Table 34).

Table 33 Supported DDR3(L) and DDR4 SDRAM Devices

Depth	Width	No. of Banks	Row Addr. Width	Col. Addr. Width
512 Mbit DDR3(L) SDRAM Devices				
32M	x16	8	12	10
64M	x8	8	13	10
1 Gbit DDR3(L) SDRAM Devices				
64M	x16	8	13	10
128M	x8	8	14	10
2 Gbit DDR3(L) SDRAM Devices				
128M	x16	8	14	10
256M	x8	8	15	10
4 Gbit DDR3(L) SDRAM Devices				
256M	x16	8	15	10
512M	x8	8	16	10
8 Gbit DDR3(L) SDRAM Devices				
512M	x16	8	16	10
1G	x8	8	16	11
2 Gbit DDR4 SDRAM Devices				
128M	x16	4	14	10
256M	x8	8	14	10

Table 33 Supported DDR3(L) and DDR4 SDRAM Devices (cont'd)

Depth	Width	No. of Banks	Row Addr. Width	Col. Addr. Width
4 Gbit DDR4 SDRAM Devices				
256M	x16	4	15	10
512M	x8	8	15	10
8 Gbit DDR4 SDRAM Devices				
512M	x16	4	16	10
1G	x8	8	16	10

Table 34 Supported LPDDR3 Devices

Depth	Width	No. of Banks	Row Addr. Width	Col. Addr. Width
1 Gbit LPDDR3 SDRAM Devices				
64M	x16	8	13	10
32M	x32	8	13	9
2 Gbit LPDDR3 SDRAM Devices				
128M	x16	8	14	10
64M	x32	8	14	9
4 Gbit LPDDR3 SDRAM Devices				
256M	x16	8	14	11
128M	x32	8	14	10
8 Gbit LPDDR3 SDRAM Devices				
512M	x16	8	15	11
256M	x32	8	15	10

17 Clock Generation Unit

The chapter describes the clock generation unit (CGU).

17.1 Features

The CGU consists of:

- An oscillator which receives either a crystal or a digital differential clock
- PLL0a generates clocks for
  - **Coherent Processing Subsystem** up to 800 MHz
  - **Quad Serial Peripheral Interfaces** reference clock up to 100 MHz
  - Supports spread spectrum clocking (SSC) with up to 0.5% down spread
- PLL0b generates clocks for
  - **Packet Switching Engine** up to 666 MHz
  - **Buffer Manager** and **Carrier Grade Quality of Service Engine** up to 500 MHz
  - **Peripherals** at 200 MHz
  - **Trusted Execution Environment** up to 500 MHz
  - Supports spread spectrum clocking (SSC) with up to 0.5% down spread
- PLL2 generates clocks for
  - **DDR SDRAM Controller** up to 533 MHz
  - Supports spread spectrum clocking with up to 0.5% down spread
- Low jitter PLL3 generates clocks for
  - **WAN SerDes** and **XFI SerDes** in Ethernet mode at 156.25 MHz
  - Precise time protocol reference time up to 500 MHz
  - Synchronous Ethernet functionality
- Low jitter PLL5 generates PON mode SerDes reference clock
- Clock dividers and Multiplexers

17.2 Functional Description

The CGU provides all necessary clock frequencies for the SoC, using a single crystal and multiple PLLs/dividers/multiplexers to generate the required clocks.

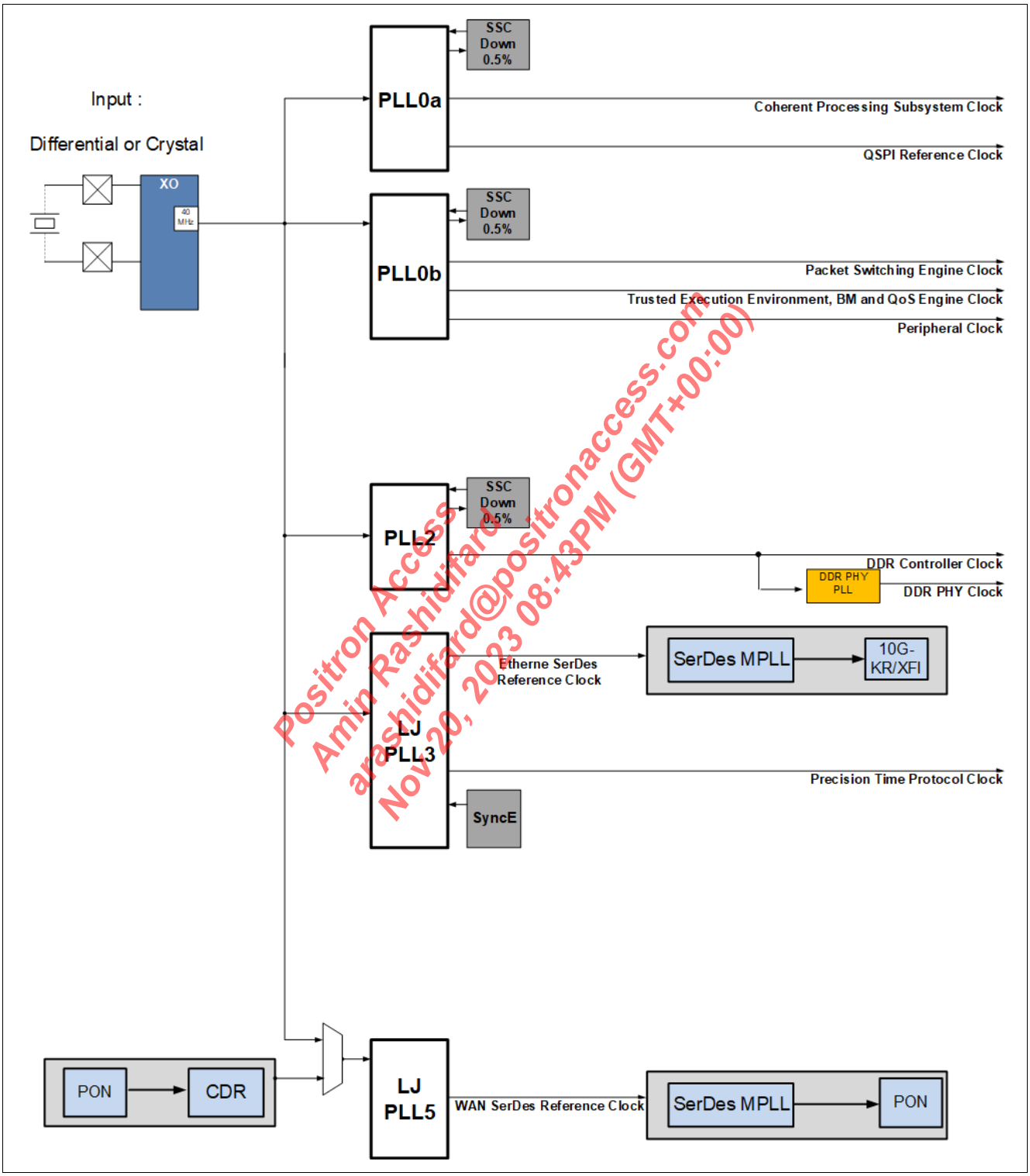


Figure 18 Overview of the CGU

The oscillator circuitry is described in **Section 17.2.1**.

17.2.1 Clock Input Option and Oscillator Circuit

The oscillator circuit is designed to work with either an external crystal or an external clock source. An oscillator circuit basically consists of an inverting amplifier with XTAL1 as input and XTAL2 as output. An AC-coupled shaper stage provides 50% duty cycle. The CLK_MD pin defines which option to use during power on reset.

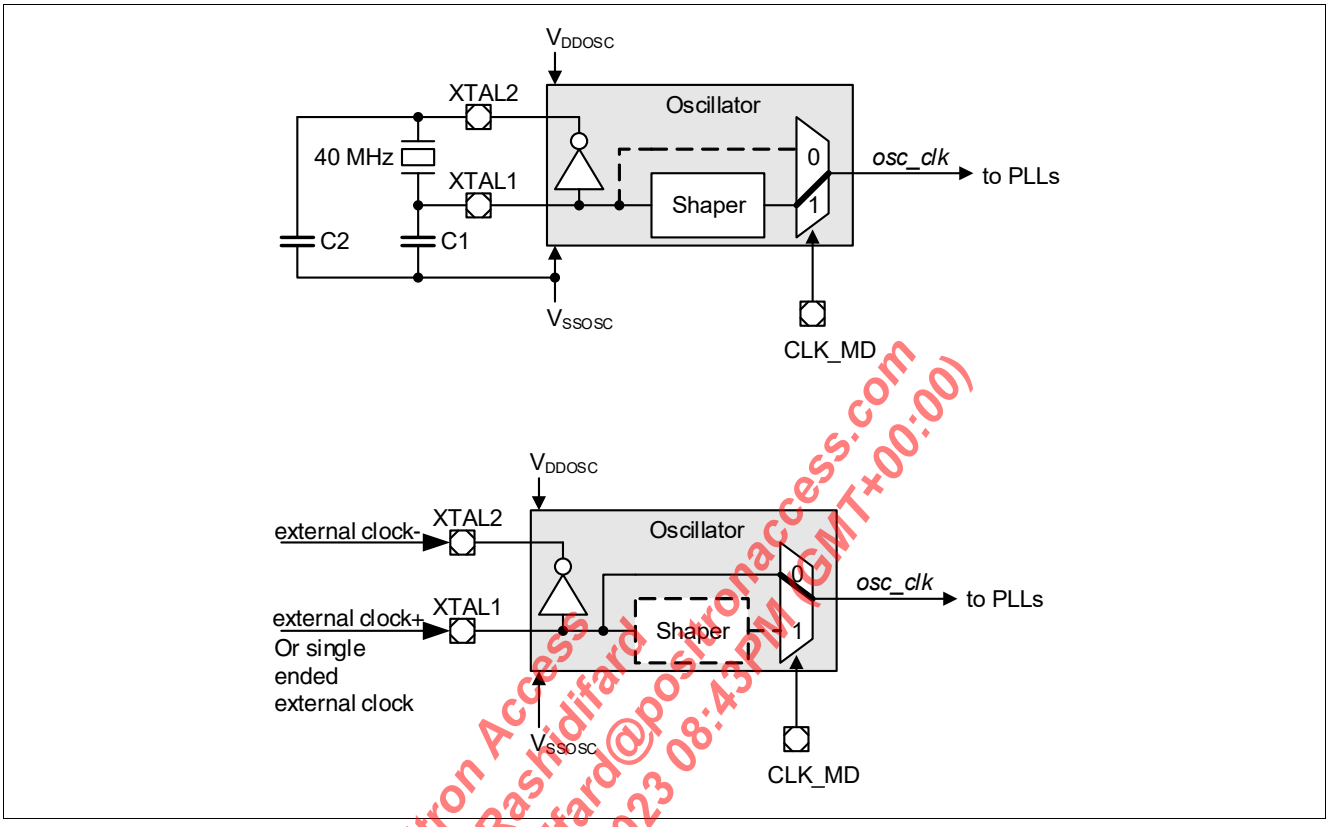


Figure 19 Clock Input Options

17.2.2 External Clock Output or Input Interface

The clock generation unit provides clocks at the external pins used for multiple purpose. The clocks are selected inside the CGU by register **CGU_IF_CLK** and are available as alternative functions at GPIO pins.

It is possible to select the following clocks, which are provided at the GPIOs.

- GPC1: configurable to be one of the below
  - 40 MHz output mode: buffered XTAL clock
  - 25 MHz or 10 MHz output mode: this is a 25 MHz or 10 MHz clock output from LJ-PLL3.
  - 1.544 MHz or 2.048 MHz or 8 kHz clock or PON NTR clock: the clock is divided from LJ-PLL3 or recovered from PON TC layer.
  - Input mode: it is used for clock source of SyncE or as PPS input
- PPS: configurable to be one of the below
  - Output mode: low jitter PPS pulse with programmable frequency and width or CPU triggered pulse for reference time synchronization with other chips.
  - Input mode: it is used for reference time synchronization with other chips.

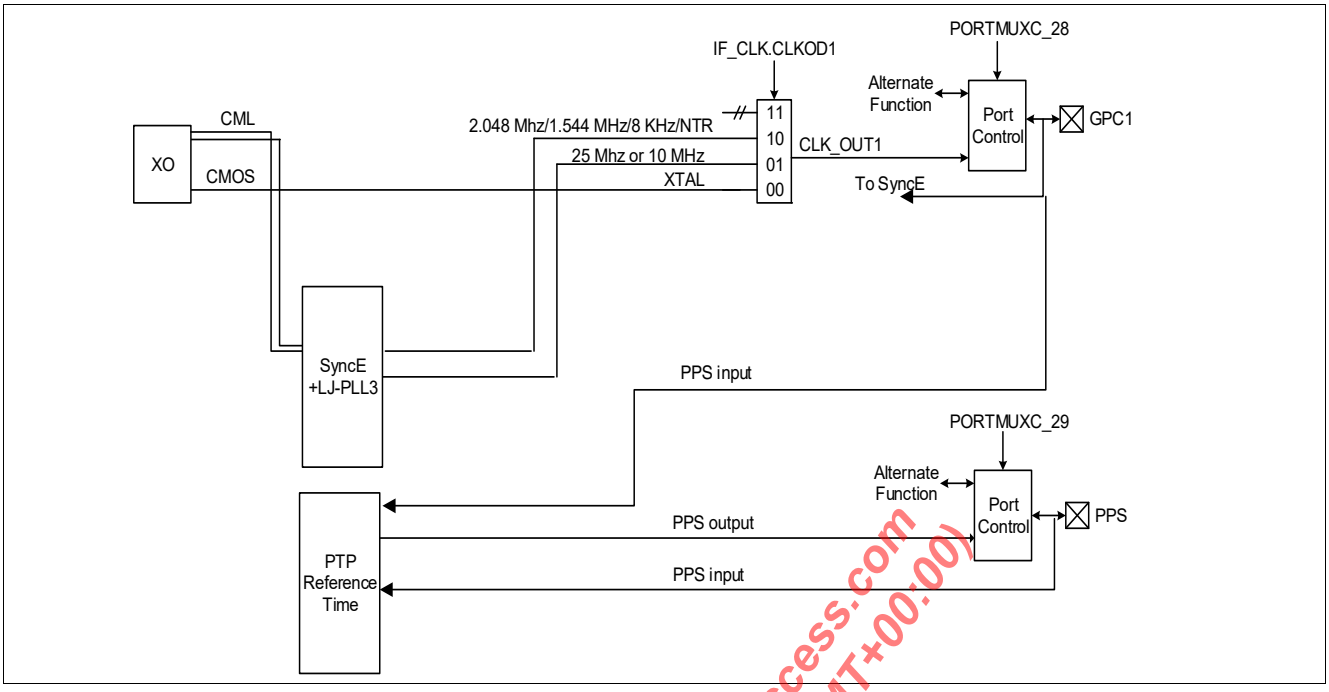


Figure 20 External Clock Output and Input Interface

17.2.3 Synchronous Ethernet

PRX126 supports Synchronous Ethernet (SyncE).

It is configurable to synchronize to one of the below clock sources.

- Recovered received clock by WAN SerDes (PON mode, AON mode and copper wire mode)
- Recovered received clock by System side SerDes
- Input clock via GPC1
- Programmable bandwidth 0.1 Hz, 3 Hz and 100 Hz

The following functions are clocked from the synchronized clock.

- WAN SerDes (PON mode, AON mode and copper wire mode)
- System side SerDes
- 1588/PTP timers
- Output clock via GPC1

Loss of signal detection is integrated on chip and all the modules are supplied seamlessly with clocks generated from the local source when the external master clock signal is not available.

17.2.4 Time of Day

PRX126 provides the Time-of-Day (ToD) network synchronization as defined by the ITU-T G.984.3 Amend. 2 and G.984.4. The ToD concept assumes that the OLT has an accurate real time clock used for network synchronization purposes. PRX126 also provides a local real time clock which is synchronized using the OMCI messages exchanged between the OLT and the ONU carrying the time of day information and an expected PON superframe counter information which is finally compared with the downstream received superframe counter information. The time-of-day distribution within the OMCI channel does not need to be in real time.

Based on the local real time clock, PRX126 derives a high precision Pulse Per Second (PPS). This pulse per second is optionally output on pin PPS and has a configurable active high pulse width. The positive edge of the 1 PPS signal exactly defines the time-of-day information carried within a message which is forwarded via the UART interface. In other words, the ToD message represents the exact time of the rising edge of the 1 PPS signal. This ToD message is sent out once per second.

18 Reset System

This chapter describes the reset system.

18.1 Features

The reset system supports:

- Power-on reset generation
  - Power-on reset input pin
  - Under voltage detection (UVD)
- Software reset requests and reset domains
- One 32-bit non-resettable register for software usage
- Watchdog timer (WDT) reset request and reset domain
- Reset control unit with finite state machine controlling the reset flow

18.2 Functional Description

The reset system mainly consists of two parts, the power-on reset logic as well as the reset control unit (RCU). The power-on reset logic controls the pin strapping functionality. Additionally, the reset system provides a reset output pin. Further, the system on chip implements components, which trigger the RCU. This is the watchdog timer (WDT). The software forces the RCU to generate a global reset request as well as individual reset requests per peripheral.

18.2.1 Overview

Figure 21 shows an overview of the reset system.

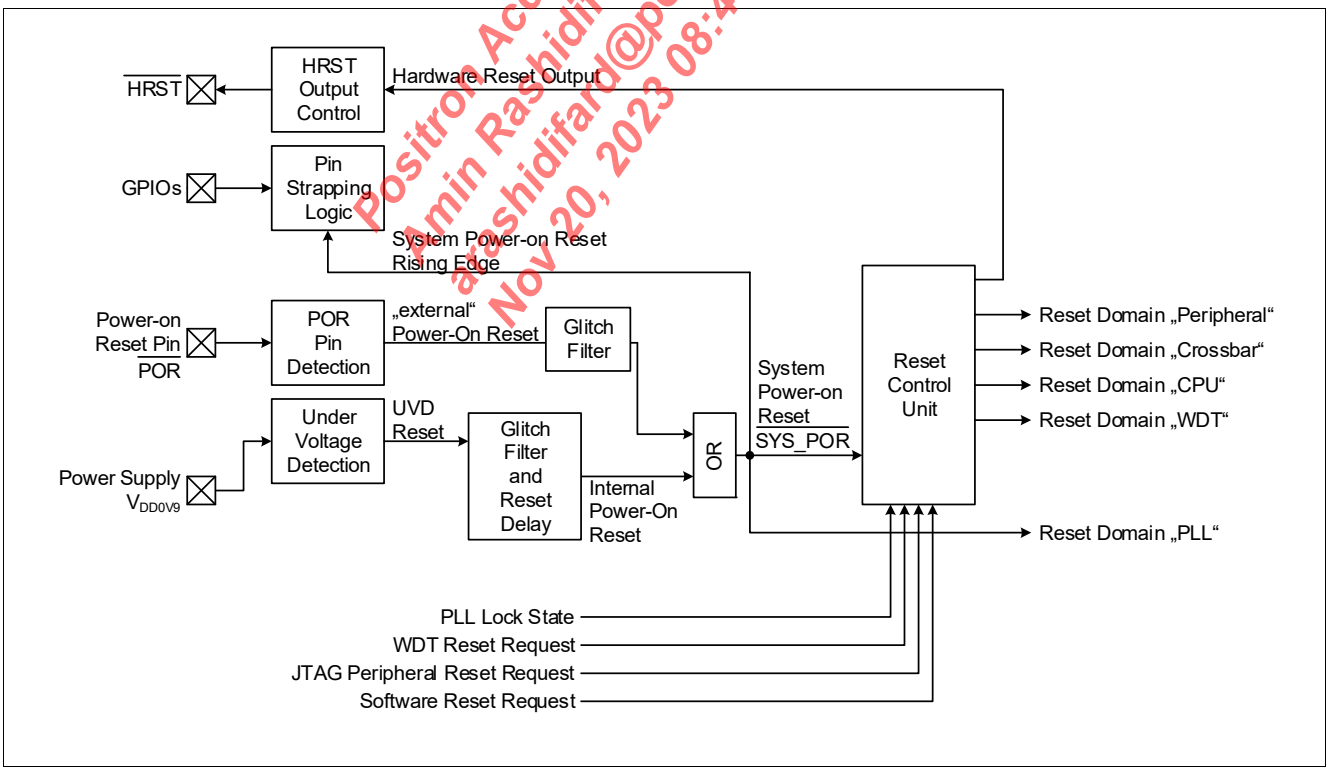


Figure 21 Reset System

18.2.2 Power-on Reset Generation

The active-low system power-on reset $\overline{\text{SYS\_POR}}$ is generated by these events:

- An active-low level at the external power-on reset input pin $\overline{\text{POR}}$
- Internally by an under voltage detection

The system power-on reset $\overline{\text{SYS\_POR}}$ forces these actions:

- Activates the reset domain PLL
- Latches the pin strap information
- Activates the general hardware reset
- Activates the hardware reset output pin $\overline{\text{HRST}}$

When the system power-on reset, $\overline{\text{SYS\_POR}}$ has been executed, these status bits are affected:

- The indication bit RST_STAT.POR is set
- All other reset cause indication bits in RST_STAT.XX are cleared
- All peripheral reset status bits in register RST_STAT.XX for all reset domains are set

18.2.2.1 Power-on Reset Generation by Input Pin $\overline{\text{POR}}$

The external power-on reset input pin $\overline{\text{POR}}$ is an active-low input pin with an internal pull-up resistor. The glitch filter logic suppresses glitches at input pin $\overline{\text{POR}}$. A low-level at input pin $\overline{\text{POR}}$ generates the system power on reset $\overline{\text{SYS\_POR}}$.

The external power-on reset input pin $\overline{\text{POR}}$ is left open, when using the internal sources under voltage detection (UVD) only. Furthermore, a need for external resistor and capacitor components at input pin $\overline{\text{POR}}$ is eliminated. The input pin $\overline{\text{POR}}$ is pulled up internally, and therefore inactive in this case.

18.2.2.2 Power-on Reset Generation by Under Voltage Detection

The UVD logic monitors the core voltage level, V_{DD0v9}, works as follows.

- An on-chip comparator compares a reference voltage, V_{REF}, and V_{DD0v9}. When VDD falls below a predefined threshold, the UVD reset signal is asserted. The glitch filter suppresses spikes of less than 20 µs.

The internal power on reset output of the UVD logic is always enabled. Finally, the reset delay element prolongs the UVD reset request for up to 120 ms.

18.2.2.3 Pin Strapping Functionality

The configuration input pins of the system-on-chip, the strap pins, are sampled and latched with the rising edge of the system power-on reset $\overline{\text{SYS\_POR}}$. This affects these registers and status bits associated with the pin strapping functionality.

- Latches the values at the GPIOs (including flash interface power supply information) into GP_STRAP
- Latches the boot information into RST_BOOT.INFO
- Latches the endianness information into RST_STAT.ENDIAN

18.2.3 Hardware Reset Output Pin

The hardware reset output pin $\overline{\text{HRST}}$ is an open-drain output with internal pull-up resistor. Pin $\overline{\text{HRST}}$ is used to force a reset of external board components, while the system-on-chip is in reset state. Additionally, pin $\overline{\text{HRST}}$ is activated by software.

The hardware reset output pin $\overline{\text{HRST}}$ is driven active-low upon these events:

- The system power-on reset $\overline{\text{SYS\_POR}}$ is activated (e.g. a system power up event happened)
- Setting the global software reset request bit RST_REQ.SWRST or WDT events
- Setting the reset request bit RST_REQ.HRST

19 Multi-Processor System

The multi-processor system (MPS) module is used for OS communication via shared memory.

The symmetric multi-processors (SMP) are single address space processors. As the two processors operating in parallel share data, they need to coordinate when operating on shared data. This coordination is called synchronization and is performed by lock variables, also named semaphores.

The shared data resides in the external DDR SDRAM. In addition, the MPS provides a SRAM used to exchange pointers via a mailbox. Therefore, this internal SRAM is named mailbox memory.

The multi-processor system provides these features:

- 1 KB SRAM for mailbox memory
- Multi-processor binary semaphores
- Interrupt requests functionality
- MPS register

The Multi-processor System provides the means to generate interrupt requests. Each CPU core is enabled to trigger interrupt requests directed to the other CPU core. The interrupt request functionality directs interrupt requests from CPU0 to CPU1 and vice versa. When the MPS interrupt signals are connected to GIC, it serves any two of the fours virtual CPUs (or VPEs).

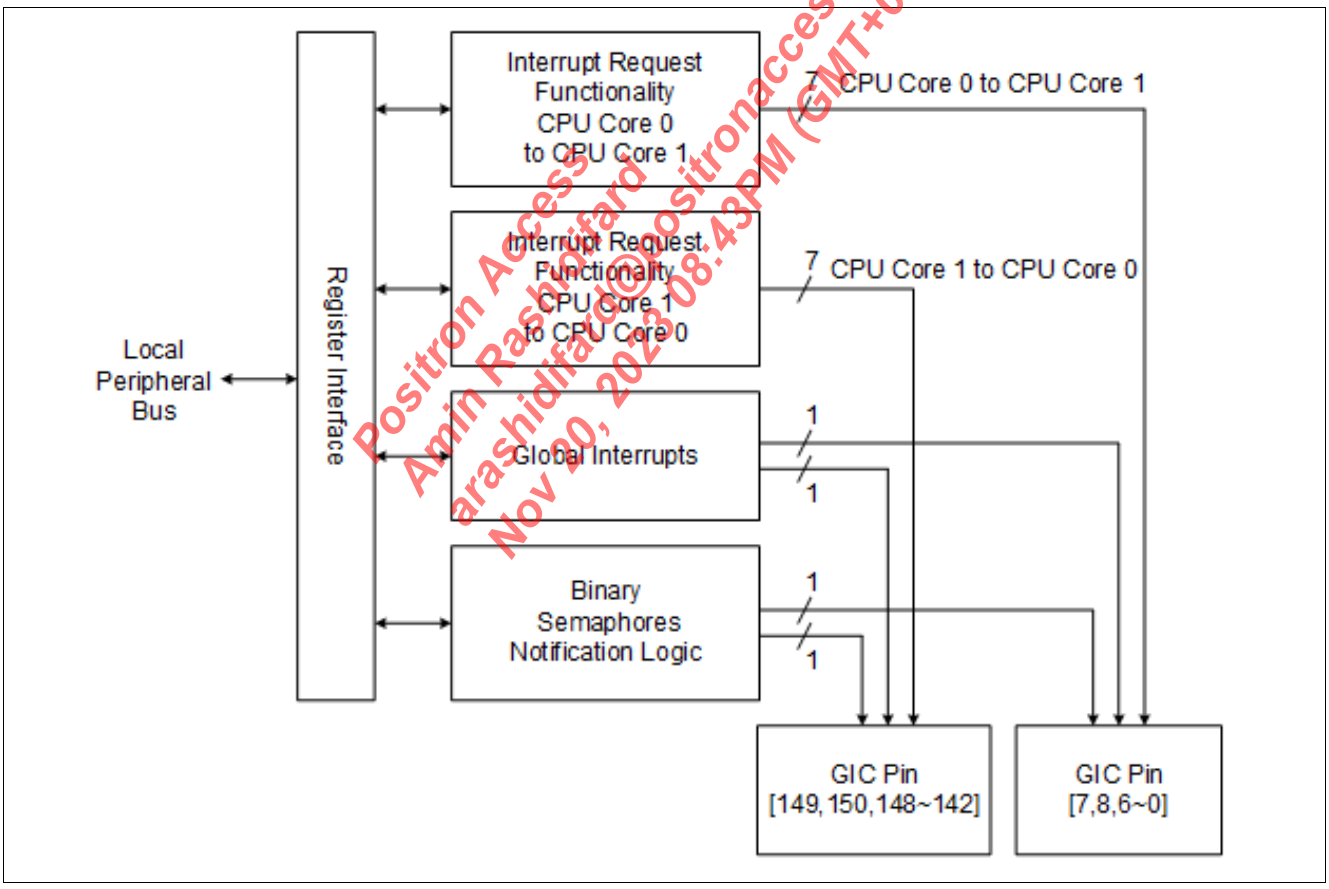


Figure 22 MPS Interrupt Request Functionality

MPS2 is used for communication between the InterAptiv* processors and the boot/TEP processor.

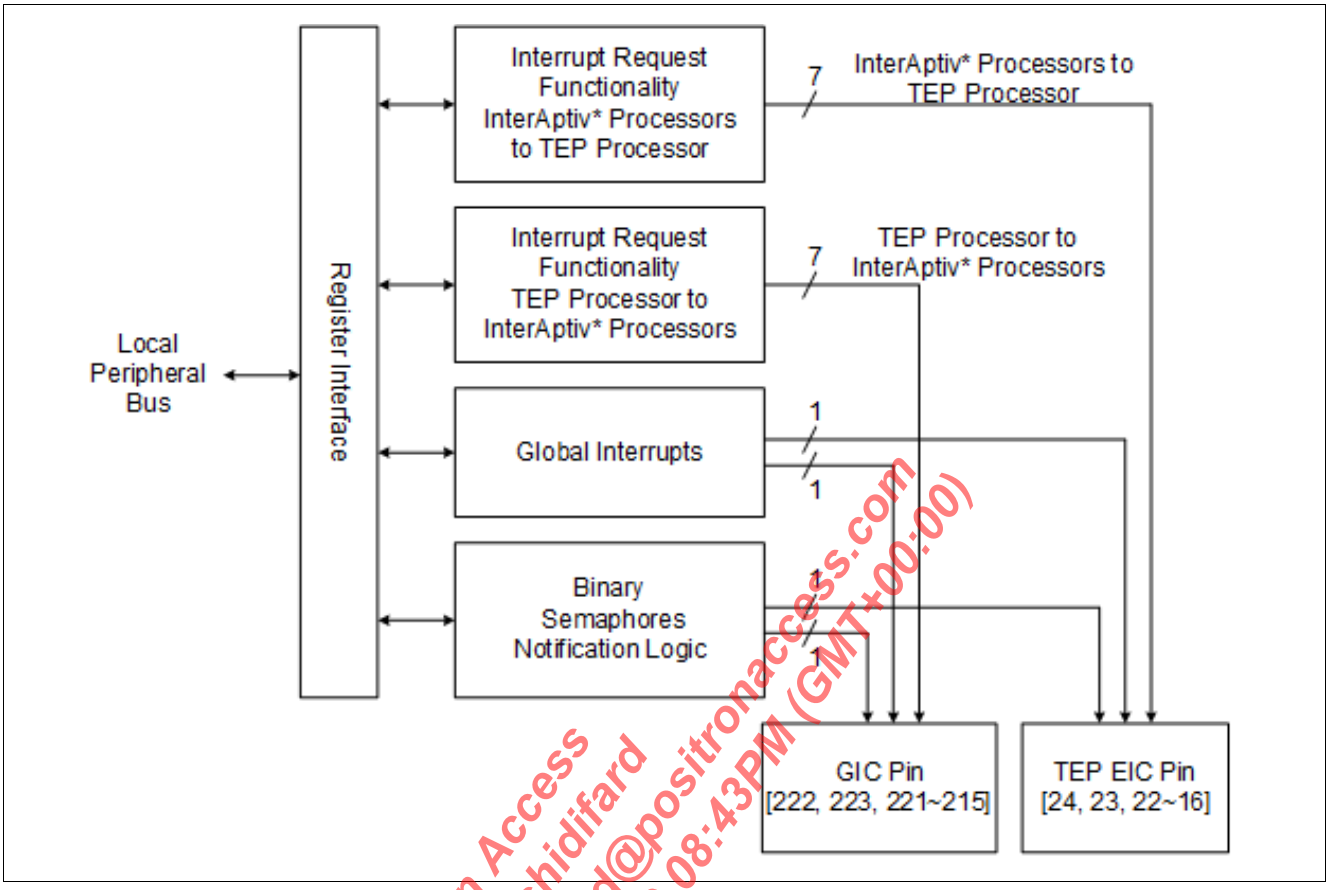


Figure 23 MPS2 Interrupt Request Functionality

20 Chip ID

The chip ID for both PRX126B0BI and PRX126B1BI devices is identical: 10004113_H.

The chip ID for PRX126B2BI is 20004113_H.

The chip ID for PRX126B3BI is 30004113_H.

The register address to read out chip ID is $1F107344_H$.

Table 35 Chip ID Fields

Fields	Bits	Description
VERSION	31:28	**Chip Version Number** 001_B **B0B1** B0 and B1 version 010_B **B2** B2 version 011_B **B3** B3 version
PNUM	27:12	**Part Number** **PRX126** PRX126 part number
MANID	11:1	**Manufacturer ID** The JEDEC normalized manufacturer ID code is 89_H.
V1	0	This bit is fixed to 1.

21 Peripherals

This chapter describes:

- **Universal Asynchronous Receiver/Transmitter** (**Chapter 21.1**)
- **Quad Serial Peripheral Interface** (**Chapter 21.2**)
- **I²C Controller** (**Chapter 21.3**)
- **General Purpose Timer Counter** (**Chapter 21.4**)
- **General Purpose I/O** (**Chapter 21.5**)
- **Dying Gasp Detection Module** (**Chapter 21.6**)
- **UART Debug Interface** (**Chapter 21.7.1**)
- **JTAG Interface** (**Chapter 21.7.2**)
- **On-chip Packet Buffer** (**Chapter 21.8**)

21.1 Universal Asynchronous Receiver/Transmitter

There are two identical asynchronous serial channel (ASC) modules integrated in the chip. Each of the ASC module is primarily used as UART and consists of the modules shown in **Figure 24**.

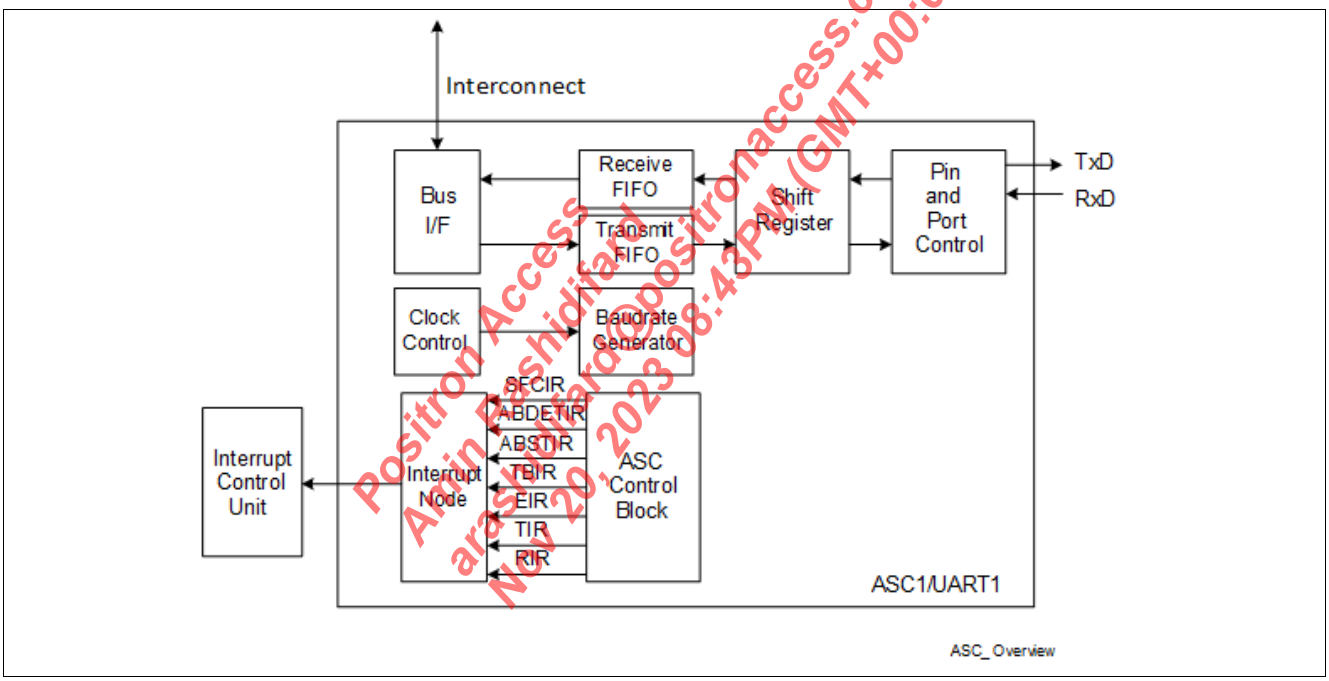


Figure 24 ASC/UART System Block Diagram

21.1.1 Features

The ASC module provides the following features.

- Automatic clock shut on/off, depending on line and/or bus activity
- Full-duplex asynchronous operating modes
  - 7- or 8-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baudrate from 12.6 MBaud to 426 Baud (at 200 MHz module fixed clock)
- Programmable XON/XOFF flow control
  - XON and XOFF characters programmable
  - Automatic flow control can be programmed, so that XON/XOFF characters are automatically inserted into/removed from the data stream, depending on the FIFO status

- Line break detection
- Programmable end-of-message detection based on character matching or time-out
- Multiprocessor mode for automatic address/data byte detection
- Loopback capability
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmitter buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receiver buffer full condition
  - On an error condition (frame, parity, overrun error, line break)
  - On XOFF reception on modem control/status signal changes
- Autobaud detection unit for asynchronous operating modes
  - Detection of standard baud rates
    1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, and 230400 Baud
  - Detection of non-standard baud rates
  - Detection of asynchronous modes
  - 7-bit, even parity; 7-bit, odd parity
    8-bit, even parity; 8-bit, odd parity; 8-bit, no parity Automatic initialization of control bits and baudrate generator after detection
  - Detection of a serial two-byte ASCII character frame
- FIFO
  - 16 X 8 receive FIFO (RXFIFO), 8-bit organized for ASC1
  - 16 X 8 transmit FIFO (TXFIFO), 8-bit organized for ASC1
  - Independent control of RXFIFO and TXFIFO depth and width
  - 8-bit FIFO data width without segmentation or reassembly in 8-bit configuration
  - Programmable receive/transmit interrupt trigger level
  - Receive and transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

21.2 Quad Serial Peripheral Interface

The quad serial peripheral interface (SPI) is equipped with a receive as well as a transmit FIFO with eight entries each 32-bit width. The QSPI control and status registers are explicitly accessed via the bus. The CPU handles bidirectional data traffic on the QSPI interface via another bus.

21.2.1 Features

The QSPI supports:

- 1 bit SPI interfaces, compliance to legacy SPI standard, mode 0
- Support single, dual or quad I/O operations
- Support double data rate operation, also called double transfer rate
- Maximum 100 MHz for single data rate
- Maximum 100 MHz for double data rate
- Adaptive delay tabs for high speed interface access timing with proven integrated DLL designed for double data rate interface
- Programming sequence to adapt different SPI flash type
- eXecution in place, fully memory mapped access for CPU
- Auto boot support for Spansion* and Macronix* devices
- Embedded 256x32 bit SRAM

21.3 I²C Controller

There is one I²C master controller (I2C0) and two I²C slave controllers (I2C1 and I2C2) integrated in chip.

21.3.1 Features

The I²C bus is a simple 2-wire serial communication bus. An I²C master is the device which initiates a data transfer on the bus and generates the clock signals to permit the transfer. At any given time, only one master is present on the bus, any device addressed is considered a slave. The master also terminates the transfer.

- I²C bus specification V2.1 compliant
- 100 Kbit/s and 400 Kbits/s speed modes are supported
- Total bus load up to 400 pF
- 8 bits per byte and data is transferred MSB first
- Operation in 7-bit or 10-bit addressing mode
- 8 stages FIFO depth (32-bit width)

Limitation of Multiple Masters in Single I²C Bus

However, when there are multiple masters in the same I²C bus, the embedded I²C master will issue dummy address cycle after a re-start phase when SOPE=0 and last data of current packet is received. This could potentially hang the bus when the dummy address is incidentally same as one of the I²C slave addresses on the same bus.

21.3.2 Features of the I²C Slave Controller

The I²C bus is a simple 2-wire serial communication bus. An I²C slave is the device which responds to a data transfer on the bus. Two I²C slave device addresses are supported by two I²C slave controllers.

The I²C slave interface is emulated on pin GPIO10 (for I2C_SCL) and GPIO11 (for I2C_SDA). GPIO mode must be selected when these two pins are used for I²C slave interface.

EEPROM emulation is supported.

- I²C bus specification V2.1 compliant
- 100 Kbit/s speed modes (0~100 Kbaud range) and 400 Kbit/s speed modes (0~400 Kbaud range) supported
- Total bus load up to 400 pF
- 8 bits per byte and data is transferred MSB first
- Operation in 7-bit addressing or 10-bit addressing mode

21.4 General Purpose Timer Counter

There are three identical GPTC modules integrated.

21.4.1 Features

Each GPTC provides the following features.

- 6 16-bit Timers
- 3 single timer/counter blocks (timer1,2,3) consisting of two 16-bit timer/counter blocks (A, B)
- Operation as two separate timer/counter blocks in 16-bit mode or a single concatenated timer/counter in 32-bit mode
- Programmable counting direction
- Run/stop control allows to stop and restart the timer/counter by software at any time
- Software controlled reload allows to restart at the current value or at the reload value
- Auto reload function enables cyclic timer/counter operation
- Operation as timer or as counter
- Programmable edge detection of external count input or level sensitive counting

- Programmable inversion of the external input is either synchronized, to count asynchronous events at 1/2 of the GPTC clock frequency, or unsynchronized, for clock-synchronous events up to the GPTC clock frequency
- Interrupt generation at overflow

21.4.2 Overview

Figure 25 shows the overview and GPTC alternate input sources of the 8 kHz clock.

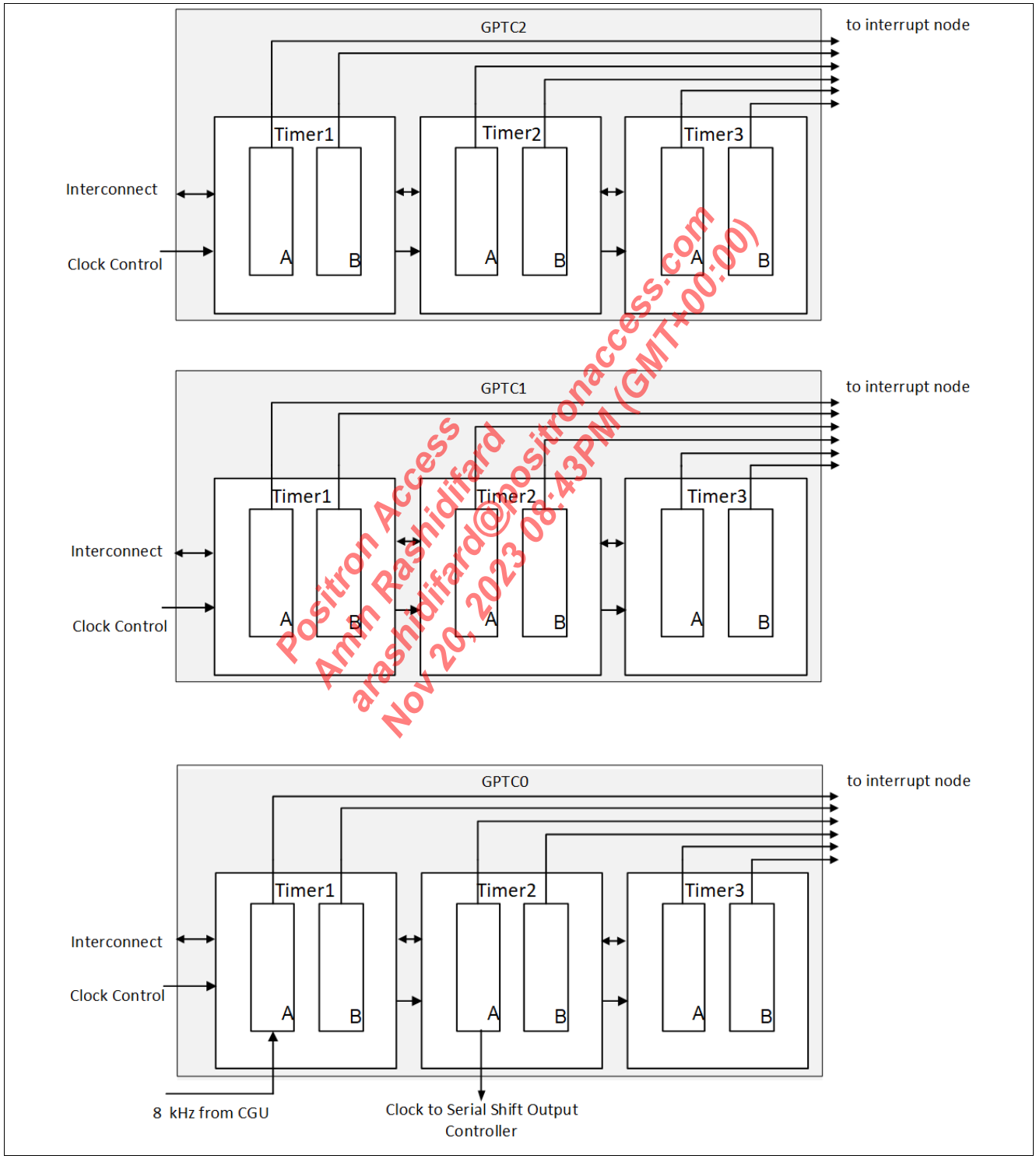


Figure 25 GPTC0/1/2 Alternate Input Source

21.5 General Purpose I/O

The module includes four parallel general purpose input/output (GPIO) ports.

21.5.1 Features

The GPIO ports support:

- Up to 24 general purpose I/Os
- Each GPIO pin can be interrupt input
- GPIO programming support bit-wise write (no need read-modify-write)
- Input/output selectable
- Input function
  - Tristate
  - High-impedance with a weak pull-up device
  - High-impedance with a weak pull-down device
  - Schmitt-trigger detection (always enabled)
- Output Functions
  - Push-pull (optional pull-up or pull-down)
  - Open drain with a weak internal pull-up
  - Open drain with an external pull-up

21.5.2 GPIO Functionality

Figure 26 shows a general block diagram of a port line. Each port line is equipped with a number of control and data bits, enabling very flexible usage of the line.

Each port pin is either configured for input or output operation. In input mode (default after reset), the output driver is switched off (high-impedance). The actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via the read only register Px_IN. In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. For GPIO function, switching between input and output mode is accomplished through the Px_DIR register, which enables or disables the output driver. When the same pin used for other alternative function, the output driver may be controlled by the function module.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used as general purpose output, the multiplexer is switched by software to the output data register Px_OUT. Software sets or clears the bit in Px_OUT, and therefore directly influences the port pin state. When the on-chip peripheral units use the pin for output signals, alternate output lines are switched via the multiplexer to the output driver circuitry.

The latch Px_IN is provided for input functions of the on-chip peripheral units. Its input is connected to the output of the input Schmitt-Trigger. Further, it is possible to connect an input signal directly to the various inputs of the peripheral units (AltDataIn). The function of the input line from the pin to the input latch Px_IN and to AltDataIn is independent of the port pin operating as input or output. This means that when the port is in output mode, the pin level is either read by software via latch Px_IN or used as an input by a peripheral. This offers additional advantages in an application.

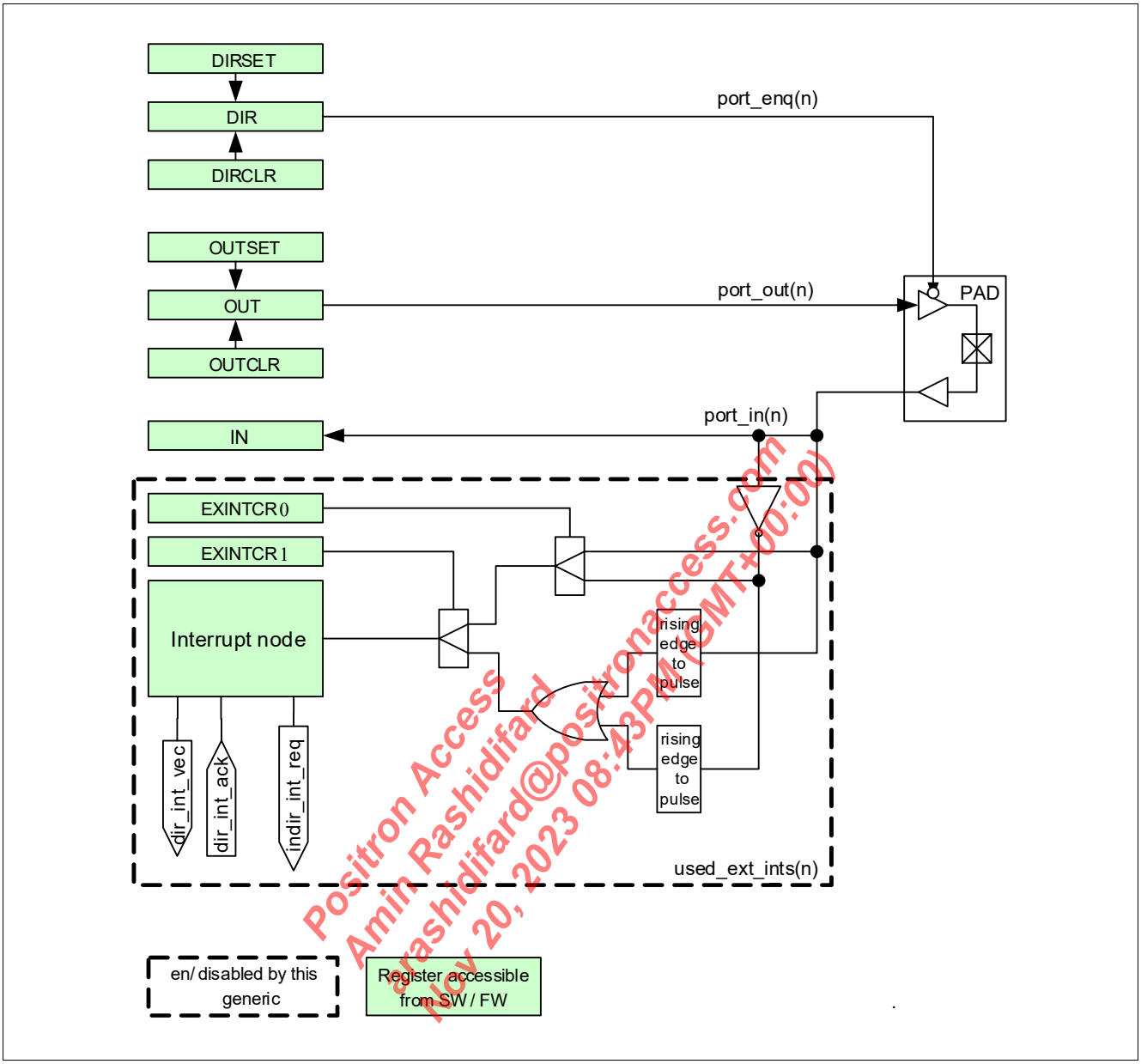


Figure 26 GPIO Bit

21.5.3 Pad Control Overview

This section provides the software/firmware interface for the static pad control for up to 32 pads.

Per Pad Features

- Pull-up enable
- Pull-down enable
- Slew rate control (1-bit)
- Drive current control (2-bit): 2, 4, 8 or 12 mA
- Pad multiplexer control (up to 3-bit)

21.5.4 External Interface

Attention: The pin functionality in Table 36 highlighted in bold indicates the pin functionality after reset.

Table 36 GPIO Functions

GPIO Pin	Pin Functionality	Associated Register/Module	Alternate Function	Direction Control
0	**GPIO used as input**	GPIO	**PORTMUXC_00**:000	**DIR_0**
	GPIO used as output			
	QSCK used as output	QSPI	010	Fixed
1	**GPIO used as input**	GPIO	**PORTMUXC_01**:000	**DIR_0**
	GPIO used as output			
	QSCS used as output	QSPI	010	Fixed
2	**GPIO used as input**	GPIO	**PORTMUXC_02**:000	**DIR_0**
	GPIO used as output			
	QSIO0 used as input	QSPI	010	Controlled by QSPI
3	**GPIO used as input**	GPIO	**PORTMUXC_03**:000	**DIR_0**
	GPIO used as output			
	QSIO1 used as input	QSPI	010	Controlled by QSPI
4	**GPIO used as input**	GPIO	**PORTMUXC_04**:000	**DIR_0**
	GPIO used as output			
	QSIO2 used as input	QSPI	010	Controlled by QSPI
5	**GPIO used as input**	GPIO	**PORTMUXC_05**:000	**DIR_0**
	GPIO used as output			
	QSIO3 used as input	QSPI	010	Controlled by QSPI
8	**GPIO used as input**	GPIO	**PORTMUXC_08**:000	**DIR_0**
	GPIO used as output			
10	**GPIO used as input**	GPIO	**PORTMUXC_10**:000	**DIR_0**
	GPIO used as output			
	I2C1_SCL as input	I2C1 and I2C2	000	**DIR_0**
11	**GPIO used as input**	GPIO	**PORTMUXC_11**:000	**DIR_0**
	GPIO used as output			
	I2C1_SDA as input	I2C1 and I2C2	000	**DIR_0**
13	**GPIO used as input**	GPIO	**PORTMUXC_13**:000	**DIR_0**
	GPIO used as output			
15	**GPIO used as input**	GPIO	**PORTMUXC_15**:000	**DIR_0**
	GPIO used as output			
16	**GPIO used as input**	GPIO	**PORTMUXC_16**:000	**DIR_0**
	GPIO used as output			

Table 36 GPIO Functions (cont'd)

GPIO Pin	Pin Functionality	Associated Register/Module	Alternate Function	Direction Control
20	**GPIO used as input**	GPIO	**PORTMUXC_20**:000	**DIR_0**
	GPIO used as output			
	OPT_RX_LOS as input	PON TC	010	Fixed
21	**GPIO used as input**	GPIO	**PORTMUXC_21**:000	**DIR_0**
	GPIO used as output			
	OPT_TX_DIS_SFP as input	PON TC	010	Controlled by PON TC
22	**GPIO used as input**	GPIO	**PORTMUXC_22**:000	**DIR_0**
	GPIO used as output			
	OPT_TX_FAULT as input	PON TC	010	Fixed
23	**GPIO used as input**	GPIO	**PORTMUXC_23**:000	**DIR_0**
	GPIO used as output			
	OPT_TX_SD used as input	PON TC	010	Fixed
24	**GPIO used as input**	GPIO	**PORTMUXC_24**:000	**DIR_0**
	GPIO used as output			
	OPT_TX_PUP used as input	PON TC	010	Controlled by PON TC
25	**GPIO used as input**	GPIO	**PORTMUXC_25**:000	**DIR_0**
	GPIO used as output			
	OPT_RX_SD_SFP used as input	PON TC	010	Controlled by PON TC
26	**GPIO used as input**	GPIO	**PORTMUXC_26**:000	**DIR_0**
	GPIO used as output			
	I2C0_SCL used as input	I2C0	010	Controlled by I2C0
27	**GPIO used as input**	GPIO	**PORTMUXC_27:** 000	**DIR_0**
	GPIO used as output			
	I2C0_SDA used as input	I2C0	010	Controlled by I2C0
28	**GPIO used as input**	GPIO	**PORTMUXC_28**:000	**DIR_0**
	GPIO used as output			
	GPC1 as input	CGU	010	
	GPC1 as output			
29	**GPIO used as input**	GPIO	**PORTMUXC_29**:000	**DIR_0**
	GPIO used as output			
	PPS as input	CGU	010	
	PPS as output			

Table 36 GPIO Functions (cont'd)

GPIO Pin	Pin Functionality	Associated Register/Module	Alternate Function	Direction Control
30	**GPIO used as in/output**	GPIO	**PORTMUXC_30**:000	**DIR_0**
	GPIO used as output			
	UART1_RX as input	UART1	001	Fixed
	UART1_RX_PON as input	PON TC	010	Fixed
	UART_RX_TEP as input	Secure TEP	100	Fixed
	UART_RX_QoS as input	QoS	101	Fixed
	UART0_RX_PON as input	PON TC	110	Fixed
31	**GPIO used as in/output**	GPIO	**PORTMUXC_31**:000	**DIR_0**
	GPIO used as output			
	UART1_TX as output	UART1	001	Fixed
	UART1_TX_PON as output	PON TC	010	Fixed
	UART_TX_TEP as output	Secure TEP	100	Fixed
	UART_TX_QoS as output	QoS	101	Fixed
	UART0_TX_PON as output	PON TC	110	Fixed

21.6 Dying Gasp Detection Module

The dying gasp monitors the external input pin (VDD_DG) and generates the interrupt to processor and to PON TC module whenever the voltage level is lower than the predefined level.

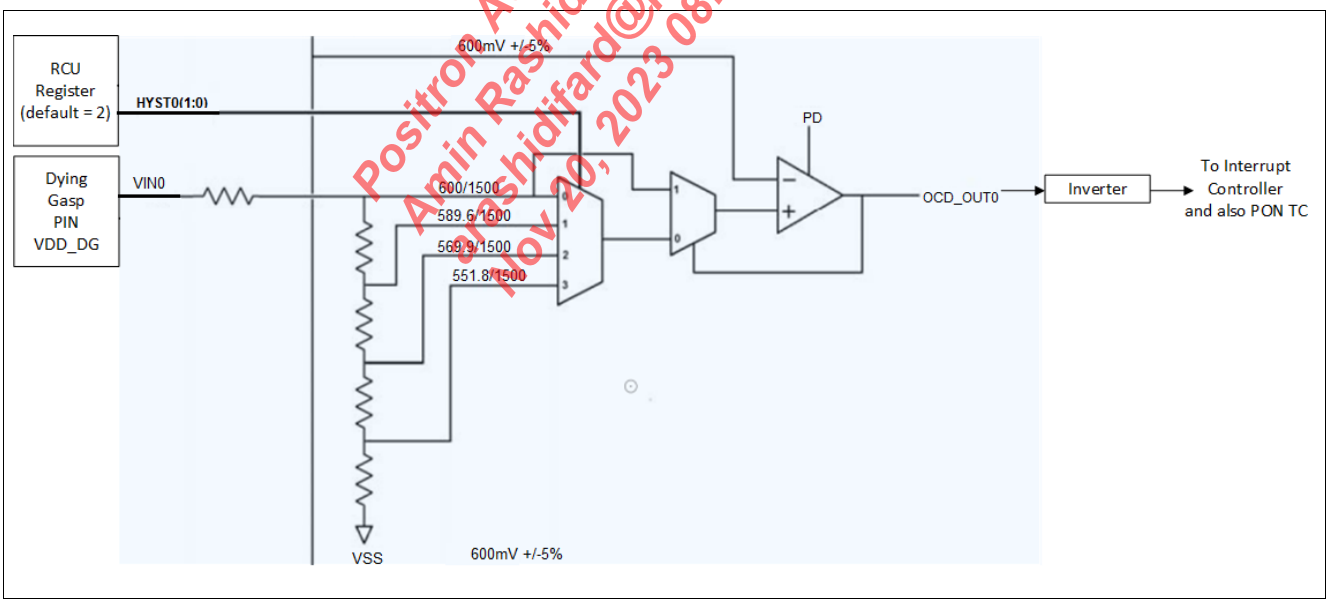


Figure 27 Block Diagram of Dying Gasp Detection

21.7 Debug Interface

There are two types of debug interfaces:

- **UART Debug Interface**
- **JTAG Interface**

21.7.1 UART Debug Interface

Two UART instances in the SoC are used for coherent processor cores debugging.

Apart from the two UART instances in the SoC, these modules have embedded UART for debugging purpose:

- Secure boot core
- QoS engine
- PON subsystem

There are two sets of UART external interfaces. Two SoC UART instances and the UART instances in the listed modules are multiplexed to these two UART external interfaces. Only two processors are debugged at the same time. See **UART Signals** for all UART interface multiplexing.

21.7.2 JTAG Interface

The TDO line is pin strapped to latch test or debug select information, whether to perform JTAG test or other internal debug access functions via the JTAG interface. Upon de-asserting $\overline{\text{TRST}}$, the level applied at TDO is latched and controls the multiplexer.

The strap pin for JTAG multiplex uses:

- 0 = Reserved - Used for internal purposes only
- 1 = JTAG test

21.8 On-chip Packet Buffer

The integrated on-chip packet buffer has the size of 7 Mbits.

The complete memory or a part of memory are used for data packet storage. The on-chip packet buffer is managed by the free segment queue manager (FSQM) inside the buffer manager (BM).

A part of memory is configured for other purposes.

22 Power Management

PRX126 supports advanced power management to control both active and idle mode power consumption.

These features are supported:

- Dynamic voltage scaling
- Two instances of PVT sensors to support thermal management and dynamic voltage scaling
- Adaptive and static clocking frequency scaling and clock gating
- Smart on-chip and off-chip buffer allocation to save chip and system power consumption

22.1 Process, Voltage and Temperature Monitor

There are two Processes Voltage and Temperature (PVT) monitors integrated in the chip.

The digital process speed monitor real time tracks the digital cell performance and converts the performance into 10-bit counter per process corner. With proper co-relationship between the measured counters and actual silicon performance, a range value for the counters corresponding to the fast/normal/slow processing speed is established, the software reads out the counter value and compares to the range setting, decides the achievable system clocking option, and sets the clock frequency accordingly. It also monitors the core voltage and the temperature.

The PVT sensor outputs are captured to the register and readable by the software.

There is overheat detection logic, which is enabled or disabled via the configuration. When output of PVT monitor is higher than the configured overheat on value (programmed via a 10-bit register), overheat signal is asserted. When the PVT monitor output is lower than the configured `overheat_off` value (programmable via a 10-bit register), overheat signal is de-asserted. The overheat signal is readable via a register bit. The overheat signal is maskable with the overheat interrupt mask (configurable via a register bit).

The overheat signals outputs of each PVT monitor are ORed and connected to the interrupt controller.

When overheat is detected, the processor reduces the frequencies of certain modules to lower the junction temperature of the chip.

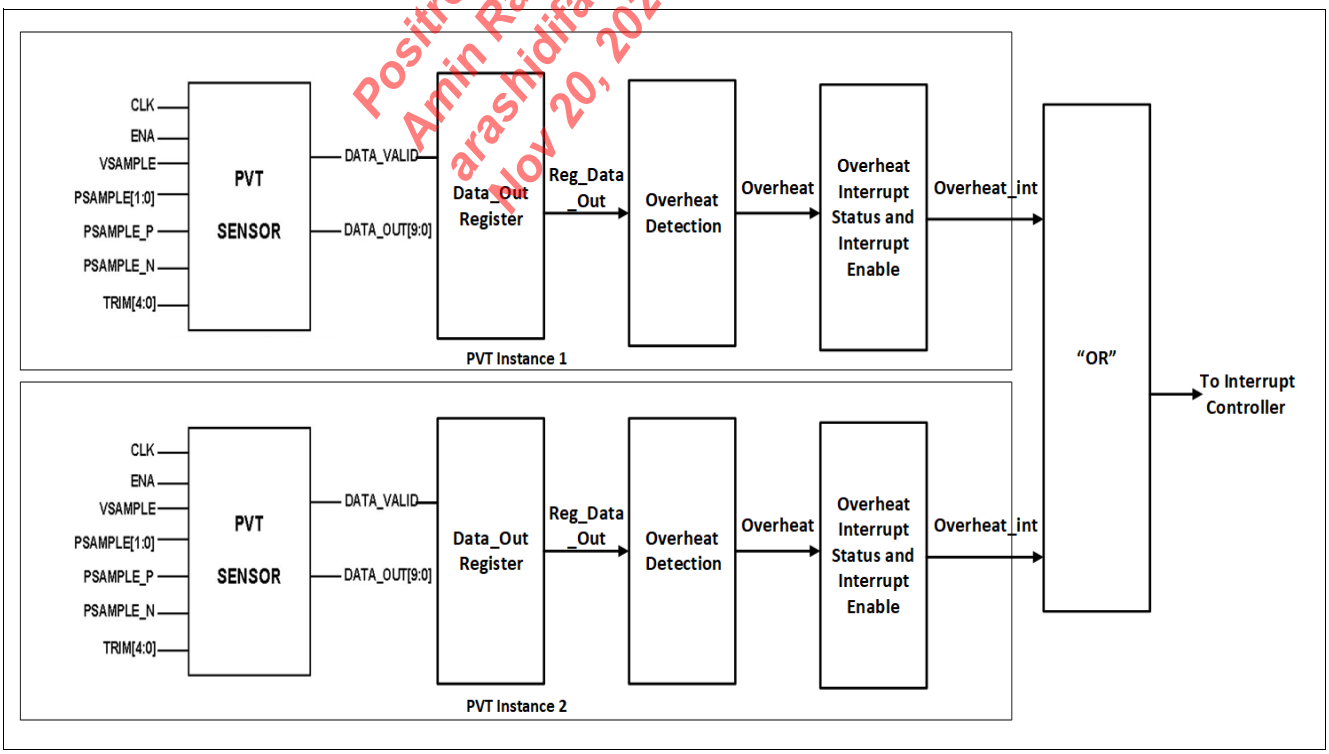


Figure 28 PVT Monitor and Overheat Detection

22.2 Dynamic Voltage Scaling

With the indications from integrated PVT sensors and the performance status from the data path hardware modules, the CPU adjusts the external power supply via the command over the I^2C master interface. Dynamic voltage scaling allows the reduction of both static leakage power and dynamic power consumption.

22.3 Adaptive and Static Frequency Scaling and Clock Gating

For unused functions in each application, the clocks are gated off via the static configuration.

The maximum frequency of the major modules is configured statically according to the performance requirements of each application.

These modules support adaptive frequency scaling and clock gating:

- Ethernet SerDes EEE modes
- Power saving modes defined by XGSPON, XGPON1, NGPON2, GPON, EPON, and 10G-EPON standards
- Packet switching engine according to the interface speed and activity
- Coherent processor core auto clocking gating and auto wake up by enabled interrupts

22.4 Smart On-Chip and Off-Chip Packet Buffer Allocation

There is an integrated 7 Mbit on-chip packet buffer. Each segment is 128-byte and this ensures the very high efficient utilization with all packet sizes. For most of time, this on-chip buffer is sufficient to store and absorb the bursts and there is no or very low activity access to DDR memory. This saves both chip and system dynamic power consumption.

23 Electrical Characteristics

The electrical characteristics describe the interface timings, power supply ranges, interface driving strength and ESD robustness.

23.1 Absolute Maximum Ratings

Table 37 lists the absolute maximum ratings.

Table 37 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{stg}	-55	–	125	°C	–
Soldering Temperature	T_{sdl}	–	–	260	°C	Compliance with Pb free reflow soldering profile as specified in J-STD-020D
Supply Voltage Core	V_{DD0v9}	-0.5	–	+0.99	V	–
Supply Voltage IO	V_{DD_IO}	-0.5	–	+3.63	V	–
Supply Voltage Analog Low	V_{AA0v9}	-0.5	–	+0.99	V	–
Supply Voltage Analog High	V_{AA1v8}	-0.5	–	+1.98	V	–
Supply Voltage DDR PAD	V_{DDQ}	-0.5	–	+1.65	V	–
Voltage on any Digital IO Pin with Respect to Ground	V_{max}	-0.5	–	V_{DD_IO} + 0.5	V	–
ESD HBM Robustness	$V_{ESD,HBM}$	–	–	1000	V	According to ANSI/ESDA/JEDEC JS-001-2014
ESD CDM Robustness	$V_{ESD,CDM}$	–	–	250	V	According to JEDEC ANSI/ESDA/JEDEC JS-002-2016

Attention: Stresses above the Max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

23.2 Operating Range

Table 38 defines the maximum values of voltages and temperature which may be applied to guarantee proper operation. These values specify the supply voltage at package pin. It considers IR drop of package bond wire and substrate trace to ensure required voltage at pad level.

Table 38 Operating Range

Parameter	Symbol	Values			Unit	Note / Summary of the voltage range
		Min.	Typ.	Max.		
Junction Temperature Absolute	T_{JABS}	-40	–	125	°C	–
Junction Temperature Operating Range	T_{JOP}	–	–	100	°C	The system thermal solution must be designed to accommodate thermal design power (TDP) within this range. Operations above the max. limit for extended periods adversely affect longterm reliability of the device.
Supply Voltage IO	V_{DD_IO}	3.13	3.3	3.47	V	3.3 V ±5 %[1]
		1.71	1.8	1.89	V	1.8 V ±5 %[1]
Supply Voltage Core	V_{DD0v9}	0.825	0.85	0.875	V	0.85 V ±3 %[2]
Supply Voltage Analog High	V_{AA1v8}	1.45	1.5	1.89	V	1.5 V -3 % to 1.8 V+5 %[3]
Supply Voltage Analog Low	V_{AA0v9}	0.825	0.85	0.875	V	0.85 V ±3 %[2]
Supply Voltage DDR3 PAD 1.5 V	V_{DDQ}	1.425	1.5	1.575	V	1.5 V ±5 %[4]
Supply Voltage DDR3L PAD 1.35 V	V_{DDQ}	1.283	1.35	1.418	V	1.35 V ±5 %[4]
Supply Voltage LPDDR3/DDR4 PAD 1.2 V	V_{DDQ}	1.14	1.2	1.26	V	1.2 V ±5 %[4]
DDR Reference Supply Voltage	V_{REF}	0.49* V_{DDR_DQ}	0.5* V_{DDR_DQ}	0.51* V_{DDR_DQ}	V	–
DDR External Termination Voltage	V_{TT}	V_{VEF}-0.04	V_{VEF}	V_{VEF}+0.04	V	–
Ground	V_{SS}	0	–	0	V	–

1) V_{DD_IO} voltage ripple (AC noise peak to peak) must be less than 2.5 %. Voltage operation range includes both DC variation and AC noise.

2) V_{DD0v9} and V_{AA0v9} voltage ripple (AC noise peak to peak) must be less than 2.5 %. Voltage operation range includes both DC variation and AC noise.

3) V_{AA1v8} voltage ripple (AC noise peak to peak) must be less than 15 mV. For operation in mode ITU-T G.989 [12] and ITU-T G.9807.1 [11], the amplitude ripple must be less than 1 mVpp/MHz for VAA1V8_PLL5 and VAA1V8_PLL. Voltage operation range includes both DC variation and AC noise.

4) V_{DDQ} Voltage ripple (AC noise peak to peak) must be less than 2.5 %. Voltage operation range includes both DC variation and AC noise.

Attention: Operations above the Max. values listed here for extended periods adversely affect long-term reliability of the device.

23.3 Power Supply Sequencing

Figure 29 shows the power supply sequencing.

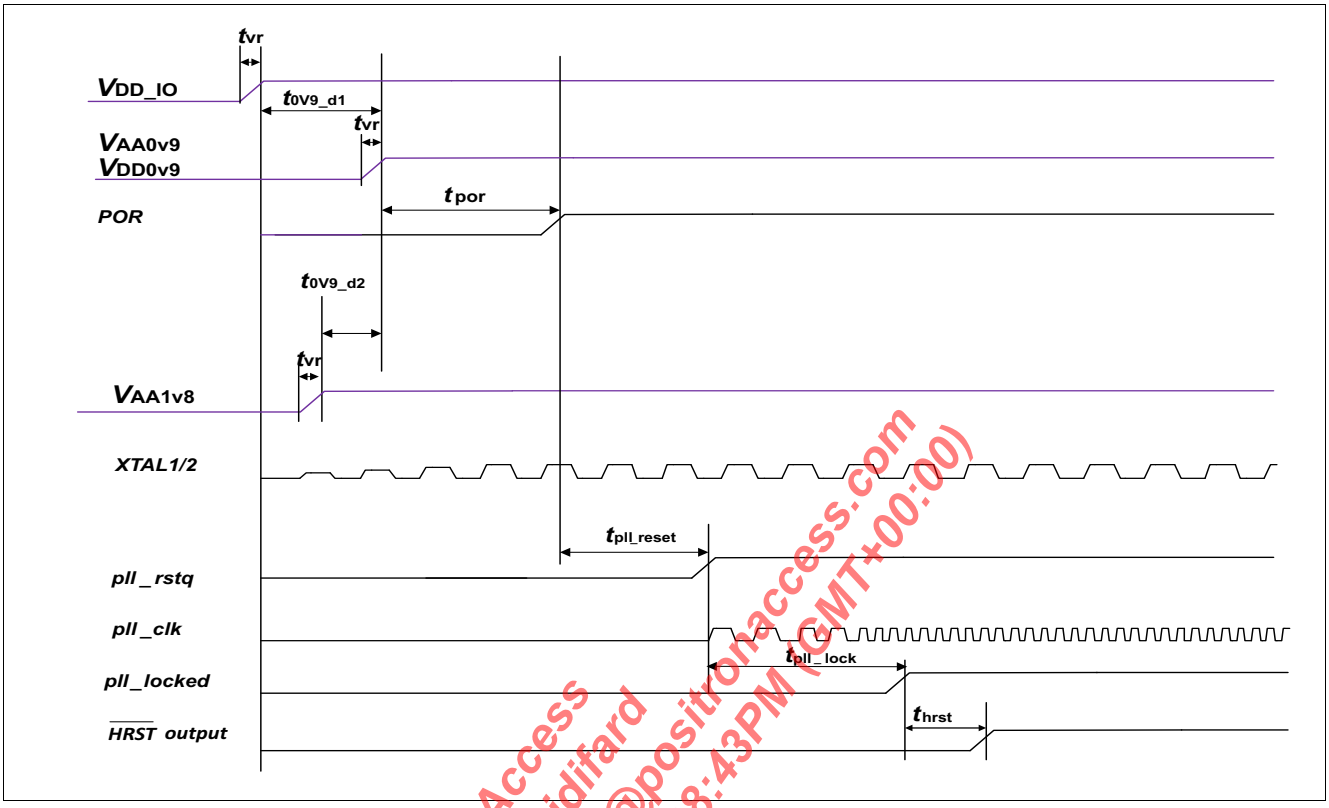


Figure 29 Power Supply Sequence

Attention: t_{pll_reset}, t_{pll_lock}, t_{hrst} are SoC internal and independent of the system design. System design is not required to achieve them.

Table 39 Timing Characteristics of Power Supply Sequence

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply VDD0V9 and VAA0V9 Ramp Up Delay Relative to VDD_IO	t_{0v9_d1}	0	–	–	ns	–
Power Supply VDD0V9 and VAA0V9 Ramp Up Delay Relative to VAA1V8	t_{0v9_d2}	0	–	–	ns	–
Power Supply Ramp Up Time	t_{vr}	10	–	–	us	–
POR Delay by Internal Under Voltage Detection	t_{por}	41	82	123	ms	–
PLL Reset after POR	t_{pll_rst}	–	8	–	us	–
PLL Lock Time	t_{pll_lock}	–	12.5	–	us	–
Reset Output Delay	t_{hrst}	–	36.8	–	us	–

23.4 Power Dissipation Overview

The power dissipation of the chip depends on the junction temperature, the device process corner, the supply voltage level, the functionality enabled, and the activity in the chip interface and inside the chip. This section describes the typical and maximum power consumption of several use cases.

These example use cases have been measured with one of the two CPU cores switched off. When enabling the second core, the power consumption increases by 75 mW (0.9 V digital core power rail).

23.4.1 Power Dissipation of Operating Idle Use Case

Table 40 describes the functionality of the operating idle use case.

Table 40 Operating Idle Use Case Description

Functionality	Mode	Rate/Load
Line Interface	XGSPON mode	FEC enabled RX Interface Speed: 9.95328 Gbit/s TX Interface Speed: 9.95328 Gbit/s
System Interface	XFI mode	RX Interface Speed: 10.3125 Gbit/s TX Interface Speed: 10.3125 Gbit/s
DDR	LPDDR3: 32-bit	Transfer Rate: 1600 MT/s Load: Application CPU access
Application CPU Core 0	Enabled	Frequency: 400 MHz Load: Single VPE with Linux* OS and OMCI management tasks
Application CPU Core 1	Disabled	NA
Traffic	No user data traffic	Load: OMCI messages only

Table 41 Operating Idle Use Case Power Dissipation

Parameters	Unit	Typical: T_J = 70 °C Typical Process Corner	Maximum: T_J = 100 °C Worst Process Corner
3.3 V Domain	mW	25	25
0.85 V Domain	mW	850	1300
1.5 V Domain	mW	270	300
DDR VDDQ Domain (Excluding External DDR Device)	mW	40[1)]	40[1)]
Total Chip Power Dissipation	mW	1185	1665
Total SFP+ Device Power Dissipation (Including all components in SFP+ device)[2)]	mW	~2400	~2800

1) In the reference board [3] External DDR device and PRX126 VDDQ share the same power rail, the power dissipation is 130 mW in total. Here it is assumed that PRX126 consumes 40 mW.

2) Refer to [3] for the detailed description of reference board of the SFP+ device.

Attention: Both typical and maximum power dissipation are measured at power supply pins with nominal voltage values.

23.4.2 Power Dissipation of Full Performance Use Case

Table 42 describes the functionality of the full performance use case.

Table 42 Full Performance Use Case Description

Functionality	Mode	Rate/Load
Line Interface	XGSPON mode	FEC enabled RX Interface Speed: 9.95328 Gbit/s TX Interface Speed: 9.95328 Gbit/s
System Interface	XFI mode	RX Interface Speed: 10.3125 Gbit/s TX Interface Speed: 10.3125 Gbit/s
DDR	LPDDR3: 32-bit	Transfer Rate: 1600 MT/s Load: Application CPU access and Data Traffic
Application CPU Core 0	Enabled	Frequency: 400 MHz Load: Single VPE with Linux* OS and OMCI management tasks
Application CPU Core 1	Disabled	NA
Traffic	Full performance data traffic	OMCI messages and 8.5Gbit/s 1518-byte bidirectional traffic Downstream short-cut data path enabled[1)]

1) See Section 3.2.1 for the description of short-cut data path.

Table 43 Full Performance Use Case Power Dissipation

Parameters	Unit	Typical: T_J = 70 °C Typical Process Corner	Maximum: T_J = 100 °C Worst Process Corner
3.3 V Domain	mW	25	25
0.85 V Domain	mW	1000	1450
1.5 V Domain	mW	270	300
DDR VDDQ Domain (Excluding External DDR Device)	mW	50[1)]	50[1)]
Total Chip Power Dissipation	mW	1345	1825
Total SFP+ Device Power Dissipation (Including all components in SFP+ device)[2)]	mW	~2600	~3000

1) In the reference board [3] External DDR device and PRX126 VDDQ share the same power rail, the power dissipation is 160 mW in total. Here it is assumed that PRX126 consumes 50 mW.

2) Refer to [3] for the detailed description of reference board of the SFP+ device.

Attention: Both typical and maximum power dissipation are measured at power supply pins with nominal voltage values.

23.5 Operating Current

Table 44 lists the operating current values.

Table 44 Operating Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DD_IO} Current	I_{IO}	–	–	50	mA	Peak current per rail to be used for power supply dimensioning. Tested with full performance at T_J = 100°C.
V_{DD0v9} and V_{AA0v9} Current	I_{0v9}	–	–	2200	mA	
V_{AA1v8} Current	I_{1v8}	–	–	250	mA	
V_{DDQ} Current (Excluding External DDR device)	I_{DDQ}	–	–	300	mA	

23.6 Digital I/O Electrical Characteristics

This section provides the digital I/O DC and AC characteristics.

23.6.1 Digital I/O DC Characteristics

Table 45 lists the digital I/O DC characteristics.

Table 45 Digital I/O DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V I/O Region						
High-Level Input Voltage	V_{IH}	2.0	–	V_{DD_IO}+ 0.3	V	–
Low-Level Input Voltage	V_{IL}	– 0.3	–	0.8	V	–
High-Level Output Voltage	V_{OH}	2.4	–	–	V	–
Low-Level Output Voltage	V_{OL}	–	–	0.4	V	–
Input Hysteresis Voltage	V_{HYS}	0.2	–	–	V	–
Input Leakage Current	I_{IL}	–	–	10	µA	
Output Leakage Current	I_{OZ}	–	–	10	µA	
1.8 V I/O Region						
High-Level Input Voltage	V_{IH}	0.65* V_{DD_IO}	–	V_{DD_IO}+ 0.3	V	–
Low-Level Input Voltage	V_{IL}	– 0.3	–	0.35* V_{DD_IO}	V	–
High-Level Output Voltage	V_{OH}	V_{DD_IO}- 0.4	–	–	V	–
Low-Level Output Voltage	V_{OL}	–	–	0.4	V	–
Input Hysteresis Voltage	V_{HYS}	0.1* V_{DD_IO}	–	–	V	–
Input Leakage Current	I_{IL}	–	–	10	µA	
Output Leakage Current	I_{OZ}	–	–	10	µA	
Internal Pull-up and Pull-down Resistor Values						
Internal Pull-up	R_{PU}	35	60	110	kΩ	–
Internal Pull-down	R_{PD}	35	58	115	kΩ	–

23.6.2 Digital I/O AC Characteristics

Timing measurements V_{TH} is made at minimum V_{IH} for a logical 1 and V_{TL} made at maximum V_{IL} for a logical 0.

Timing measurements for digital output V_{TH} are made at minimum V_{OH} for a logical 1 and V_{TL} made at maximum V_{OL} for a logical 0.

Figure 30 shows the AC testing input/output waveforms. The load capacitors are according to the specific interface standard, all non-specified interfaces use 30 pF as assumed loading.

The timings are measured at pins of PRX126.

Attention: All timing parameters specified in this release of the document may be updated based on chip characterization.

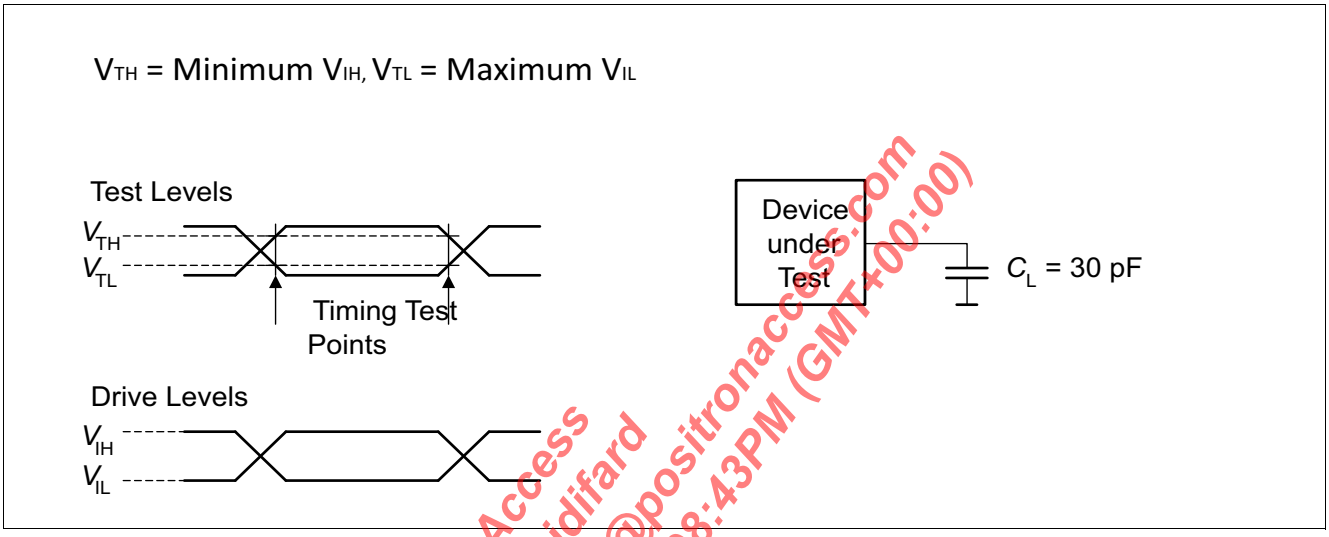


Figure 30 Input/Output Waveform for AC Tests

23.6.2.1 QSPI Interface

This section defines the QSPI Interface timings.

Attention: All timing parameters specified in this release of the document may be updated based on chip characterization.

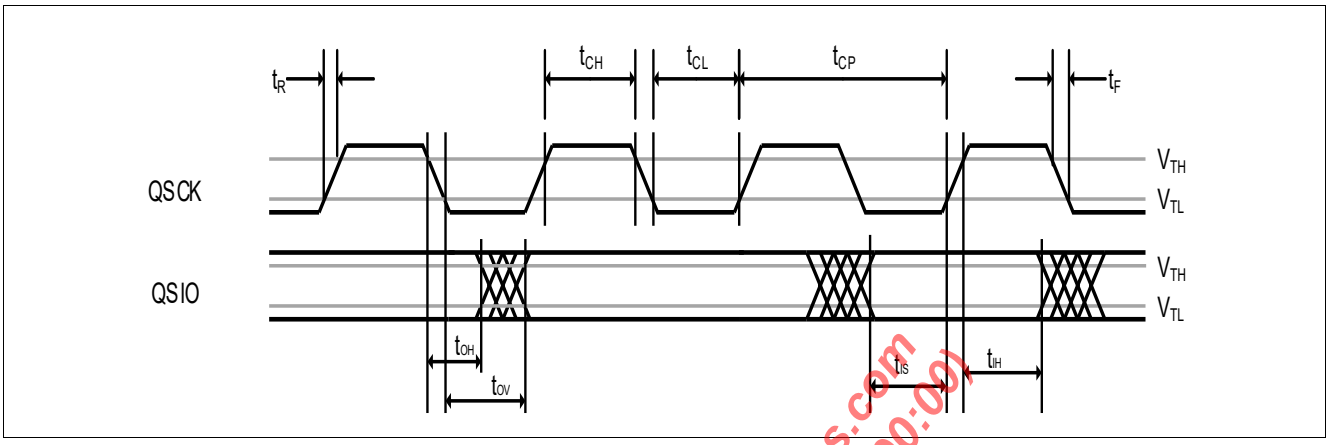


Figure 31 QSPI Interface SDR Mode Timing

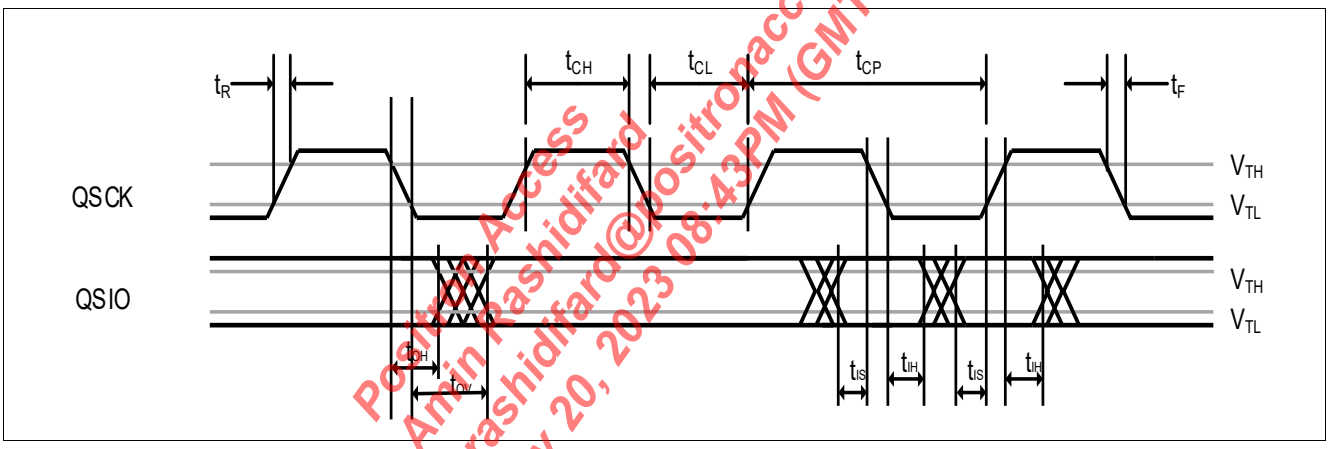


Figure 32 QSPI Interface DDR Mode Timing

Table 46 Timing Values QSPI Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
QSCK Clock Period[1)]	t_{CP}	10.0	–	–	ns	–
QSCK Duty Cycle	t_{CH}/t_{CP}, t_{CL}/t_{CP}	45	50	55	%	–
QSIO Input Setup Time	t_{IS}	3.5	–	–	ns	–
QSIO Input Hold Time	t_{IH}	0.5	–	–	ns	–
QSIO Output Valid Time	t_{OV}	–	–	5.0	ns	–
QSIO Output Hold Time	t_{OH}	0	–	–	ns	–

1) QSPI clock supports range of frequencies, up to 100 MHz.

23.6.2.2 I²C Interface

Figure 33 shows the I²C interface timing.

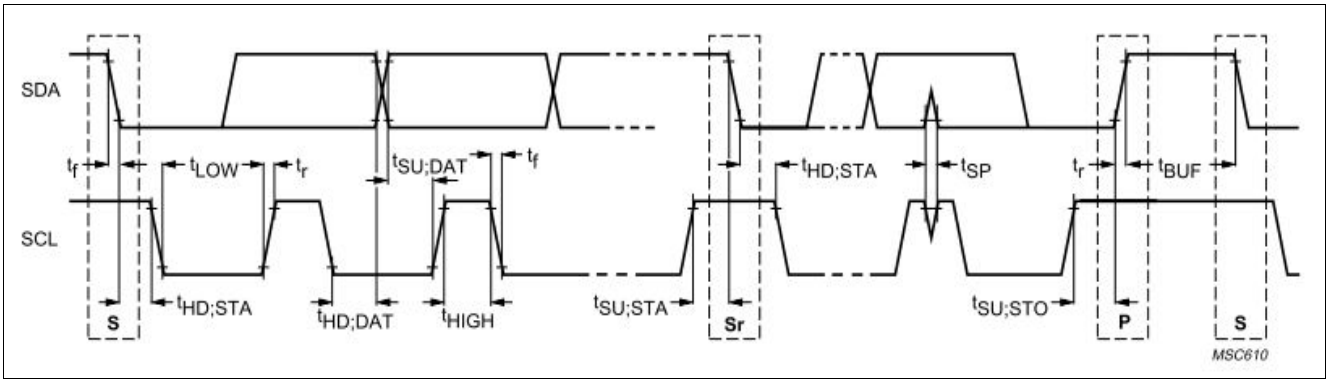


Figure 33 I²C Timing

Table 47 describes the timing values.

Attention: All timing parameters specified in this release of the document may be updated based on chip characterization.

Table 47 I²C Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Standard Mode						
SCL Frequency	f_{SCL}	0	–	100	kHz	–
Setup Time Data to Shift Clock	$t_{SU,DAT}$	250	–	–	ns	–
Hold Time Data to Shift Clock	$t_{HD,DAT}$	0	–	3450	ns	–
Setup Time START to Shift Clock	$t_{SU,STA}$	4700	–	–	ns	–
Hold Time START, STOP to Shift Clock	$t_{HD,STA/STO}$	4000	–	–	ns	–
Low Time	t_{LOW}	4700	–	–	ns	–
High Time	t_{HIGH}	4000	–	–	ns	–
Rising Time	t_r	–	–	1000	ns	–
Falling Time	t_f	–	–	300	ns	–
Bus Free Time	t_{BUF}	4700	–	–	ns	–
Fast Mode						
SCL Frequency	f_{SCL}	0	–	400	kHz	–
Setup Time Data to Shift Clock	$t_{SU,DAT}$	100	–	–	ns	–
Hold Time Data to Shift Clock	$t_{HD,DAT}$	0	–	900	ns	–
Setup Time START to Shift Clock	$t_{SU,STA}$	600	–	–	ns	–
Hold Time START, STOP to Shift Clock	$t_{HD,STA/STO}$	600	–	-	ns	–
Low Time	t_{LOW}	1300	–	–	ns	–
High Time	t_{HIGH}	600	–	–	ns	–
Rising Time	t_r	20	–	300	ns	–
Falling Time	t_f	12	–	300	ns	–
Bus Free Time	t_{BUF}	1300	–	–	ns	–

23.6.2.3 Test Interface

The test interface is used to debug the CPU.

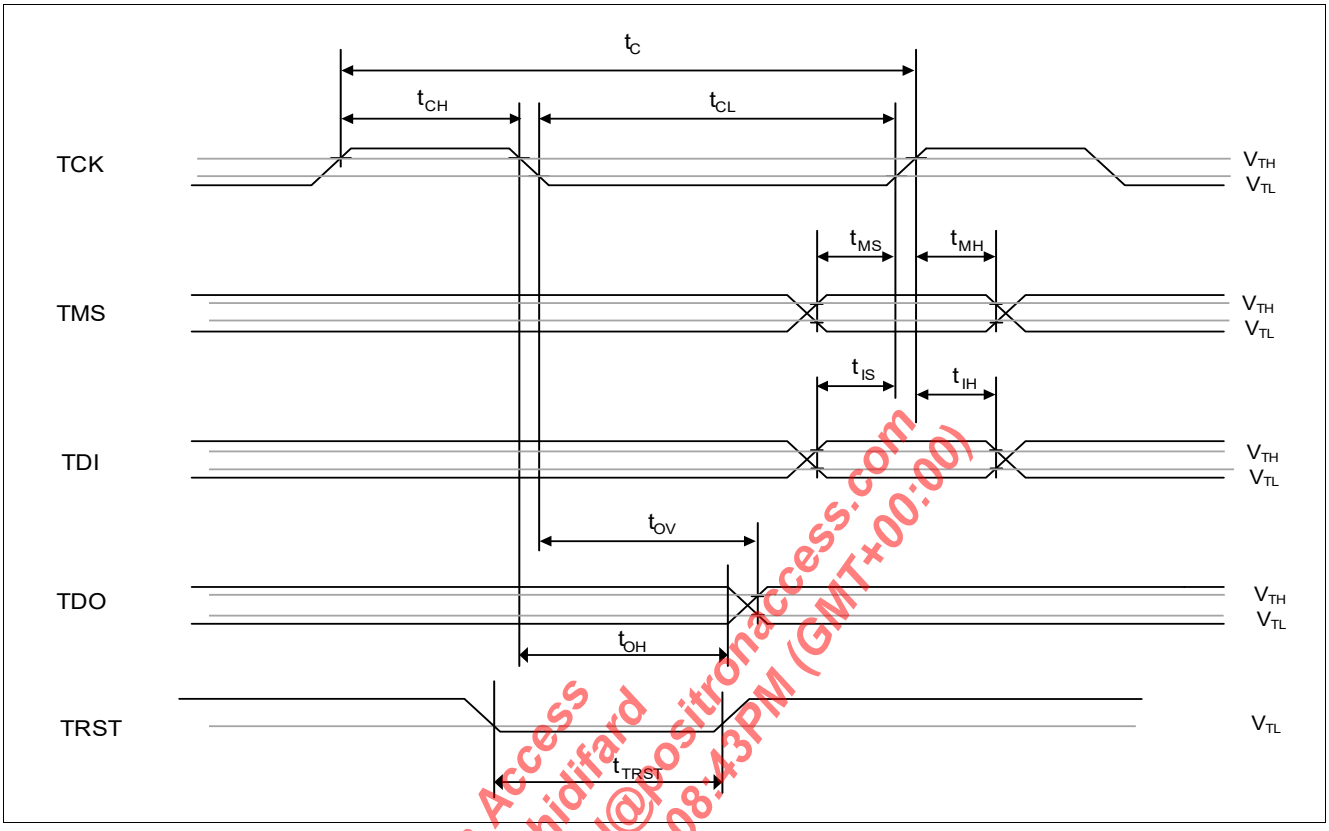


Figure 34 Test Interface Timing

Table 48 and Table 49 describe the timing values.

Attention: All timing parameters specified in this release of the document may be updated based on chip characterization.

Table 48 Test Interface Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK Clock Period	t_C	100	–	–	ns	–
TCK High Time	t_{CH}	40	–	–	ns	–
TCK Low Time	t_{CL}	40	–	–	ns	–

Table 49 JTAG Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TMS Setup Time	t_{MS}	20	–	–	ns	–
TMS Hold Time	t_{MH}	20	–	–	ns	–
TDI Setup Time	t_{IS}	20	–	–	ns	–
TDI Hold Time	t_{IH}	20	–	–	ns	–

Table 49 JTAG Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDO Valid Time	t_{OV}	–	–	20	ns	–
TDO Hold Time	t_{OH}	0	–	–	ns	–
TRST Low Time	t_{TRST}	10	–	–	ns	–

23.6.2.4 External Reset

PRX126 supports an asynchronous hardware reset POR input. **Table 50** lists the timing requirements on the POR input to the device.

Figure 35 depicts the signal sequence waveforms for better illustration of the timings. After the power-supply settling time, all primary input signals to the PRX126 must be defined. After releasing the POR, the integrated PLL locks on the reference clock and the device boots up. The Reset output pin HRST is deactivated.

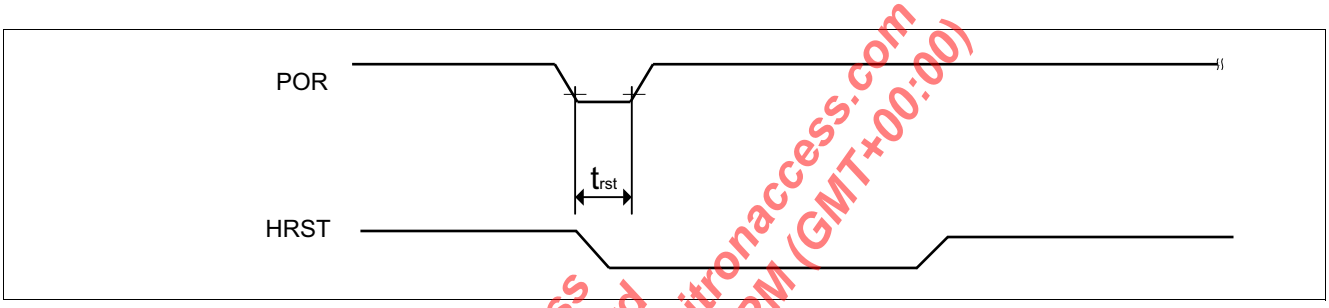


Figure 35 Timing Diagram for the External Reset Sequence

Table 50 AC Characteristics of the POR Pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Valid Reset Input	t_{rst_valid}	200	–	–	ns	The duration of low pulse on POR pin longer than this parameter can trigger the valid reset.
Invalid Reset Input	$t_{rst\_invalid}$	–	–	50	ns	The duration of low pulse on POR pin shorter than this parameter is filtered and does not trigger the reset.

23.7 DDR Interface Characteristics

This section provides the DDR interface DC and AC characteristics.

23.7.1 DDR Interface DC Characteristics

Table 51 DDR Interface DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DDR4						
I/O Supply Voltage DDR4 at 1.2 V	V_{DDQ}	1.14	1.2	1.26	V	–
High-Level Input Voltage	V_{IH}	V_{REF}+ 0.065	–	V_{DDQ}	V	–
Low-Level Input Voltage	V_{IL}	-0.3	–	V_{REF} -0.065	V	–
High-Level Output Voltage	V_{OH}	0.9* V_{DDQ}	–	–	V	–
Low-Level Output Voltage	V_{OL}	–	–	0.1* V_{DDQ}	V	–
LPDDR3						
I/O Supply Voltage LPDDR3 at 1.2 V	V_{DDQ}	1.14	1.2	1.26	V	–
High-Level Input Voltage	V_{IH}	V_{REF}+ 0.1	–	V_{DDQ}	V	–
Low-Level Input Voltage	V_{IL}	-0.3	–	V_{REF} -0.1	V	–
High-Level Output Voltage	V_{OH}	0.9* V_{DDQ}	–	–	V	–
Low-Level Output Voltage	V_{OL}	–	–	0.1* V_{DDQ}	V	–
DDR3L						
I/O Supply Voltage DDR3L at 1.35 V	V_{DDQ}	1.283	1.35	1.418	V	–
High-Level Input Voltage	V_{IH}	V_{REF}+ 0.09	–	V_{DDQ}	V	–
Low-Level Input Voltage	V_{IL}	-0.3	–	V_{REF} -0.09	V	–
High-Level Output Voltage	V_{OH}	0.8* V_{DDQ}	–	–	V	–
Low-Level Output Voltage	V_{OL}	–	–	0.2* V_{DDQ}	V	–
DDR3						
I/O Supply Voltage DDR3 at 1.5 V	V_{DDQ}	1.425	1.5	1.575	V	–
High-Level Input Voltage	V_{IH}	V_{REF}+ 0.09	–	V_{DDQ}	V	–
Low-Level Input Voltage	V_{IL}	-0.3	–	V_{REF} -0.09	V	–
High-Level Output Voltage	V_{OH}	0.9* V_{DDQ}	–	–	V	–
Low-Level Output Voltage	V_{OL}	–	–	0.2* V_{DDQ}	V	–

23.7.2 DDR Interface AC Characteristics

Refer to DDR3/DDR3L (JESD79-3F/79-3-1) [25], DDR4 (JESD79-4) [26] as well as LPDDR3 (JESD209-3C) [27] for DDR interface AC characteristics.

Table 52 DDR Device Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DDR3(L)-2133, LPDDR3-2133, DDR4-2133						
Clock Period	t_{ck}	0.937	–	–	ns	+50 ppm to -5000 ppm spectrum spread

23.8 Ethernet SerDes Interface Characteristics

This section describes the electrical characteristics of the Ethernet SerDes Interface on the PRX126. The interface is able to operate at 1.25 GT/s (SGMII/1000BASE-X), 3.125 GT/s (SGMII/2500BASE-X), and 10.3125 GT/s (XFI/SFI/10G-KR/UXSGMII).

The interface complies with Cisco* SGMII Electrical Specification [21], IEEE802.3-2012 Electrical Specification [19], SFF-8431 [23], CEI-6G and CEI-11G [18], and Universal SXGMII Electrical Specification [22].

Table 53 SerDes Transmit DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Differential Output Voltage Peak to Peak Maximum	V_{ODP2P_MAX}	900	1000	1100	mV	Differential output voltage is programmable. This is measured when maximum swing is configured.
Differential Output Voltage Peak to Peak TX Disabled	V_{ODP2P_DIS}	–	10	15	mV	–
Transition Time (20% <-> 80%)	T_T_{trans}	24	36	47	ps	–
Random Jitter	T_T_{Rj}	–	–	0.15	UI	–
Deterministic Jitter	T_T_{Dj}	–	–	0.15	UI	–
Total Jitter	T_T_{Tj}	–	–	0.28	UI	–
Differential Output Impedance	T_R_{diff}	90	100	110	Ω	–
Common Output Impedance	T_R_{cm}	45	50	55	Ω	–
Differential Mode Return Loss	T_S_{dd}	10	–	–	dB	–
Common Mode Return Loss	T_S_{cc}	10	–	–	dB	–

Table 54 SerDes Receive DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Differential Input Voltage Peak to Peak	V_{IDP2P}	50		1200	mV	–
Differential Input Impedance	R_R_{diff}	90	100	110	Ω	–
Common Input Impedance	R_R_{cm}	45	50	55	Ω	–
Differential Mode Return Loss	R_S_{dd}	10	–	–	dB	–
Common Mode Return Loss	R_S_{cc}	10	–	–	dB	–

Table 55 Board AC Coupled Capacitors

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SGMII/1000BASE-X /2500BASE-X	C_{SGMII}	–	–	4.7	nF	–
XFI/SFI/10G-KR/Single-port USXGMII	C_{XFI}	–	–	100	nF	–

Table 56 Reference Resistor

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference Resistor	R_{refres}	198	200	202	Ω	–

23.9 Power-on Reset Detection

Table 57 includes the electrical parameters of the power-on reset (POR) detection.

Table 57 POR by UVD Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Detection Threshold (0.9V)	V_{DET_POR}	0.64	–	0.68	V	5% accuracy
Delay for Activation of Reset	t_{ACT_POR}	10	20	30	us	50% accuracy
Delay for Deactivation of Reset	t_{DEACT_POR}	41	82	123	ms	50% accuracy

23.10 Dying Gasp Detection

Table 58 includes the electrical parameters of the dying gasp detection.

Table 58 Dying Gasp Detection Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Detection Threshold	V_{DET_DG}	–	1.5	–	V	5% accuracy
Hysteresis	V_{HYS_DG}	0	79	131	mV	It is programmable with 4 Hysteresis levels with 5% accuracy

23.11 Built-in Temperature Sensor

Table 59 includes the electrical parameters of the integrated temperature sensor.

Table 59 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature Range	T_{range}	-40	–	125	°C	–
Resolution	–	–	10	–	bits	–
Accuracy (Untrimmed)	–	-5	–	+5	°C	–

23.12 Crystal Specification

The crystal is attached to the PRX126 SoC and must follow the specifications found in Table 60.

Table 60 Specification of the 40 MHz Crystal

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal Frequency	F_{XTAL}	–	40	–	MHz	Oscillation mode is fundamental.
Total Frequency Stability	T_{XTAL_PPM}	-30	–	+30	ppm	Refer to sum of all effects: e.g. general tolerance, aging, temperature dependency
Series Resonant Resistance	R_M	–	–	40	Ω	–
Drive Level	P_D	0.08	0.10	0.2	mW	–
Load Capacitance	C_L	16	–	26	pF	–
Shunt Capacitance	C_0	–	–	7	pF	–

23.13 Differential Input Clock Specification

The differential clocks are input to the PRX126 SoC and must follow the specifications found in Table 61.

Table 61 Differential Input Clock Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal Frequency	F_{XTAL}	–	40	–	MHz	
Total Frequency Stability	T_{XTAL_PPM}	-30	–	+30	ppm	Refer to sum of all effects: e.g. general tolerance, aging, temperature dependency
Duty Cycle	D_{XTAL}	45	50	55	%	–
RMS Jitter	J_{RMS}	–	–	2.7	ps	–
Differential Input Voltage Single Ended Swing	V_{SWING}	200	–	900	mV	–
Single Ended Input Voltage Cross Point	V_{CROSS}	100	–	450	mV	–
Input Impedance	R_P	–	–	40	kW	–
Input Capacitance	C_P	–	–	1	pF	–

24 Package Outlines

The product is assembled in PG-VF2RBGA-287-9.4x8.6-C-1A package which complies with regulations requiring lead free material. It is ROHS 6/6 compliant.

PG-VF2RBGA: Plastic Green Very Thin Profile Flip Chip Fine Pitch Rectangle Ball Grid Array Package.

Table 62 JESD51 Thermal Resistance Package Parameter

Item	Description/Value
Package Type	PG-VF2RBGA-287-9.4x8.6-C-1A
Thermal Resistance: Junction to Case - Top	$R_{th,\ JCtop}$ = 0.08 K/W
Thermal Resistance: Junction to PCB	$R_{th,\ JCbot}$ = 11.4 K/W[1)]

1) Refer to JESD51-8.

Note: The above values are based on JEDEC standard thermal simulation condition on a 6-layer JEDEC PCB.

Table 63 JESD51-2 Thermal Resistance Package Parameter (Natural Still Air)

Item	Description/Value
Thermal Resistance: Junction to Ambient	$R_{th,\ JA}$ = 21.1 K/W
Thermal Characterization: Junction to Case - Top	Ψ_{JCtop} = 0.5 K/W[1)]
Thermal Characterization: Junction to Case - Bottom	Ψ_{JCbot} = 4.8 K/W[2)]

1) Thermal characteristic parameter referring Case-Top at the package centre top surface.
2) Thermal characteristic parameter referring Case-Bottom at the package centre BGA bottom side.

Note: The above values are based on JEDEC standard thermal simulation condition on a 6-layer JEDEC PCB. Board size: 101.5x114.5 mmx 1.0 mm; Number of Thermal Vias: 161; Ambient Temperature: 85 °C.

Table 64 Thermal Resistance Package Parameter: Compact 2-R Model Network

Item	Description/Value
Package Type	PG-VF2RBGA-287-9.4x8.6-C-1A
Thermal Resistance: Junction to Case - Top	$R_{th,\ JCtop}$ = 0.08 K/W
Thermal Resistance: Junction to Case - Bottom	$R_{th,\ JCbot}$ = 6.1 K/W

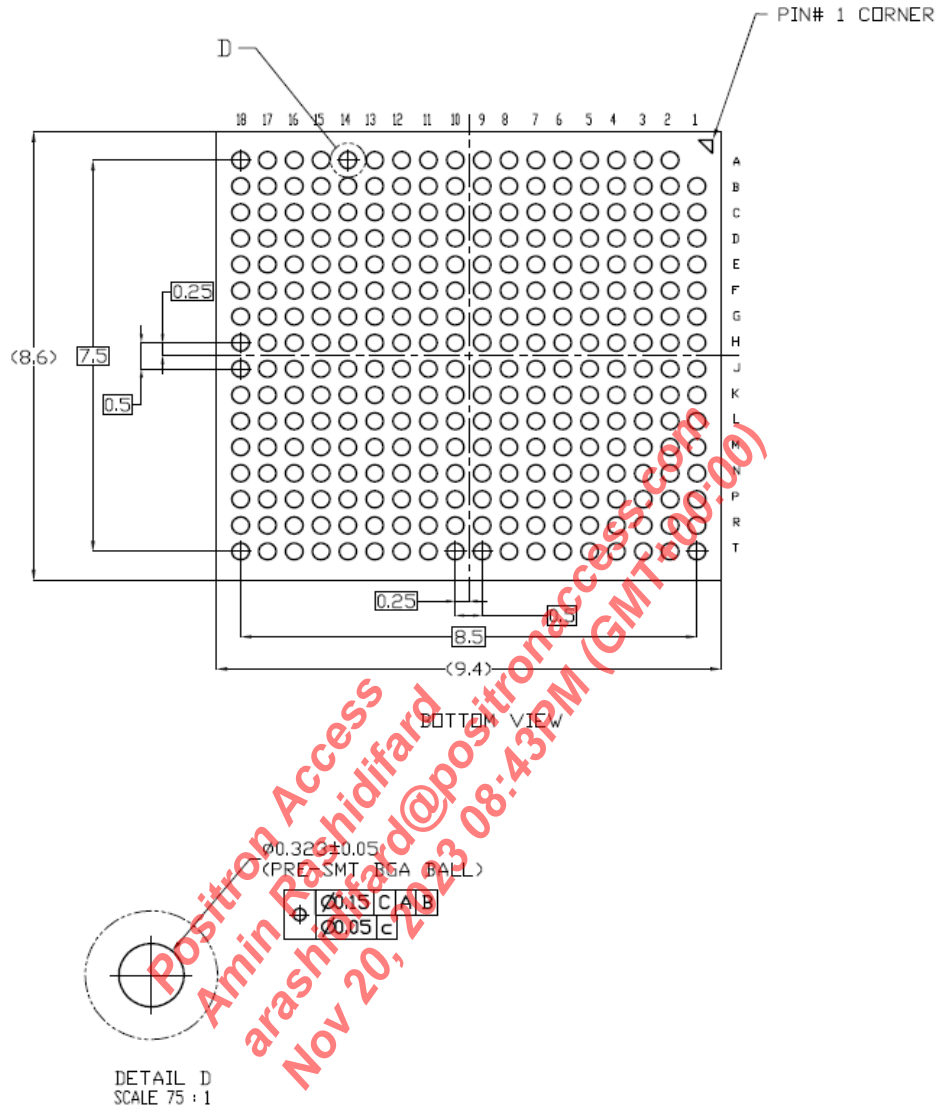


Figure 36 PG-VF2RBGA-287 (Bottom View)

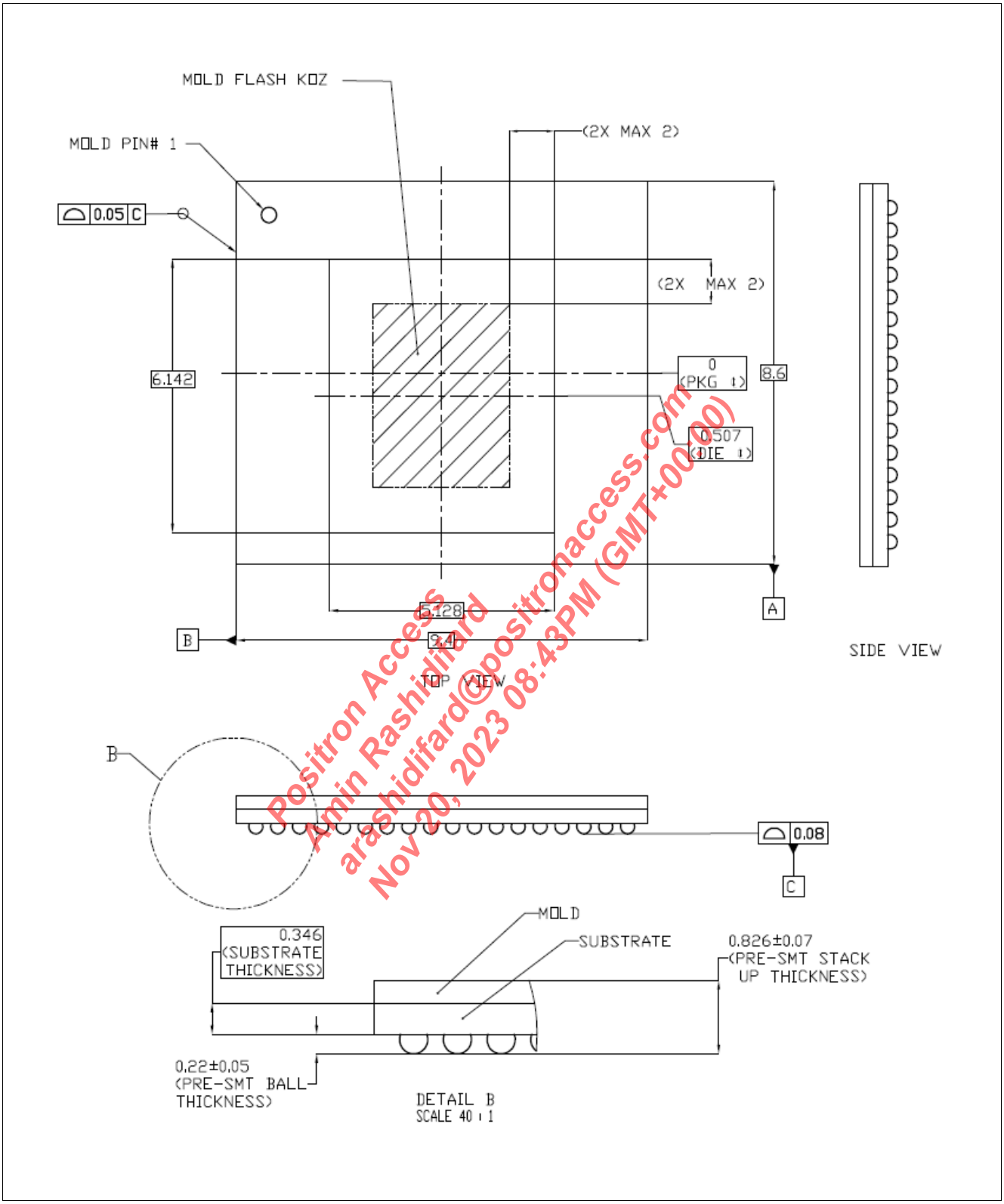


Figure 37 PG-VF2RBGA-287 (Top and Side View)

Note: The package is sourced from multiple vendors.

Refer to **[8]** for the PCB assembly recommendations.

24.1 Chip Identification and Ordering Information

Figure 38 shows an example of the marking pattern on the PRX126 device.

Note: The actual chip marking may differ slightly from the illustration.

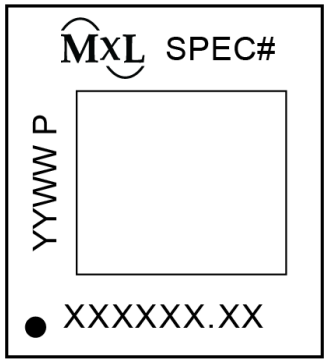


Figure 38 Example of Chip Marking

Table 65 explains the chip marking information and **Table 66** provides chip ordering information for PRX126.

Table 65 Chip Marking Pattern

Marking	Description
Text Line 1	MaxLinear Logo and Spec. Number - See **Table 66** 5-character Spec. Number until (including) PRX126B2BI 10-character Spec. Number since PRX126B3BI
Text Line 2	Date Code (YYWW) and Assembly Site Code (P)
Text Line 3	Wafer Lot Number

Table 66 Product and Package Naming

Product Name	Ordering Code	S-Spec#	Package
PRX126	999VHB	SLNEB	PG-VF2RBGA-287-9.4x8.6-C-1A
PRX126	PRX126B3BI-AV-T	PRX126B3BI	PG-VF2RBGA-287-9.4x8.6-C-1A

Terminology

A	
AES	Advanced Encryption Standard
ANSI	American National Standards Institute
AON	Active Optical Network
B	
BL	Boot Loader
C	
CM	Crypto Module
CM	Coherence Manager
CPS	Coherent Processing Subsystem
CQE	Carrier Grade **QoS** Engine
D	
DC Port	Direct Connect Port
DMA	Direct Memory Access
DSA	Digital Signature Algorithm
E	
ECC	Error Correction Code
EEE	Energy-Efficient Ethernet
EMI	Electromagnetic Interference
EP	**PCIe*** End Point
F	
FMT	Fixed Memory Translation
FSB	First Stage Bootloader
FSQM	Free Segment Queue Manager
FTTx	Fiber to the X
FXS	Foreign eXchange Subscriber interface is the port that actually delivers the analog line to the subscriber
G	
10G-KR	Backplane Ethernet 10 Gbit/s over Printed Circuit Boards
GEM	GPON Encapsulation Method
GPIO	General Purpose Input/Output
GPTC	General Purpose Timer Controller
GPON	Gigabit Passive Optical Network
H	
HSTL	High-Speed Transceiver Logic
I	
I^2C	Inter-Integrated Circuit
IA	Image Authenticator

iAptiv	interAptiv*
J	
JTAG	Joined Test Action Group
L	
LAN	Local Area Network
LED	Light Emitting Diode
LLID	Logical Link Identification
LPI	Low Power Idle
M	
MAC	Media Access Controller
MACsec	IEEE **MAC** Security Standard
MDIO	Management Data Input/Output
MPE	Multi-Core Processing Engine
N	
NG-PON2	Next Generation Passive Optical **PON**
NPU	Network Processing Unit
NTR	Network Time Reference
NVM	Non-Volatile Memory
O	
OAM	Operations, Administration, and Maintenance
OMCI	**ONU** management and control interface
ONU	Optical Network Unit
OS	Operating System
OTP	One Time Programmable Memory
P	
PCB	Printed Circuit Board
PCIe*	Peripheral Component Interconnect Express
PCS	Physical Coding Sublayer
PMAC	Pseudo Media Access Controller
PLL	Phase-Locked Loop
POE	Power over Ethernet
PON	Passive Optical Network
POR	Power on Reset
PPS	Pulse Per Second
PTP	Precise Transport Protocol
Q	
QoS	Quality of Service
QSPI	Quad Serial Peripheral Interface
R	

RC	PCIe* Root Complex
RED	Random Early Detection
RoT	Root of Trust
RTP	Real Time Transport Protocol
RX	Receive
RXAUI	10 Gigabit Reduced Attachment Unit Interface
S	
SB	Secure Boot
SBCR	Secure Boot Confidentiality Root
SFP	Small Form factor Pluggable
SHA	Secure Hash Standard
SMP	Symmetric Multi-Processing
SoC	System on Chip
SPE	Secure Platform Engine
SPI	Serial Peripheral Interface
SSC	Spread-Spectrum Clocking
SSID	Service Set Identifier
SSO	Serial Shift Output
SyncE	Synchronous Ethernet
T	
TC	Thread Context
TC	Transmission Convergence
TEE	Trusted Execution Environment
TEP	Trusted Execution Processor
TRNG	True Random Number Generator
TX	Transmit
U	
UART	Universal Asynchronous Receiver/Transmitter
UGW	Universal GateWay
USXGMII	Universal Serial 10GE Media Independent Interface
UVD	Under-Voltage Detection
W	
WAN	Wide Area Network
WDT	Watchdog Timer
Wi-Fi	Wireless Local Area Network
WoL	Wake on LAN
WRED	Weighted Random Early Detection
X	
XFI	10G Serial Electrical Interface
XGMII	10 Gigabit Media Independent Interface

XG-PON	10-Gigabit Capable Passive Optical **PON**
XGS-PON	10-Gigabit Capable Symmetrical Passive Optical **PON**
XO	Crystal Oscillator

Literature References

[1] 10G PON Chipset System Overview Rev. 3.0

[2] MIPS32 InterAptiv* Multiprocessing System Software User's Manual, Revision 01.04 or later

[3] 10G PON Development Kit EASY PRX126 REF BOARD V2.2.3 (SFP+) HW6.1.03 Hardware Design Guide Rev. 1.1

[4] 10G PON Chipset PRX126 Design Considerations Application Note Rev. 1.1

[5] 10G PON Chipset PRX126 (PRX126xxBI) Errata Sheet Rev. 5.0

[6] 10G PON Subsystem Software Overview Rev. 2.0

[7] 10G PON Subsystem Programmer's Guide Rev. 2.3

[8] P(G)-VQFN Packages PCB Assembly Recommendations Application Note Rev. 1.5

Attention: Refer to the latest revisions of the documents.

Standards References

[9] ITU-T G.984 series: Gigabit-capable passive optical networks (G-PON), including:
G.984.1: General characteristics
G.984.2: Physical Media Dependent (PMD) layer specification
G.984.3: Transmission convergence layer specification

[10] ITU-T G.987 series: 10-Gigabit-capable passive optical network (XG-PON) systems, including:
G.987.1: General Requirements
G.987.2: Physical media dependent (PMD) layer specification
G.987.3: Transmission convergence (TC) layer specification

[11] ITU-T G.9807.1: 10-Gigabit-capable symmetric passive optical network (XGS-PON)

[12] ITU-T G.989: 40-Gigabit-capable passive optical networks (NG-PON2), including:
G.989.1: General Requirements
G.989.2: Physical media dependent (PMD) layer specification
G.989.3: Transmission convergence (TC) layer specification

[13] ITU-T G.988: ONU management and control interface (OMCI) specification

[14] IEEE 802.3av Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications - Amendment: Physical Layer Specifications and Management Parameters for 10 Gb/s Passive Optical Networks10G EPON

[15] IEEE 802.1 Suite of Standards for Ethernet Networking and Bridging

[16] IEEE 1904 IEEE Standard for Service Interoperability in Ethernet Passive Optical Networks (SIEPON)

[17] BBF TR-156: Using GPON Access in the context of TR-101

[18] Common Electrical I/O (CEI): Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O (IA # OIF-CEI-02.0), OIF, February 28th 2005

[19] IEEE 802.3-2012: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications, IEEE Computer Society, 2012

[20] IEEE 802.3bz-2016 Amendment 7: Media Access Control Parameters, Physical Layers, and Management Parameters for 2.5 Gbs/s and 5 Gbs/s Operation, Types 2.5GBASE-T and 5GBASE-T, IEEE Computer Society, 2016

[21] Serial-GMII Specification, Revision 1.8, Cisco* Systems, April 27th 2005

[22] Universal SXGMII Interface for a Single MultiGigabit Copper Network Port, Revision 2.2, Cisco* Systems, November 5th 2012

[23] SFF-8431: Specifications for Enhanced Small Form Factor Pluggable Module SFP+ Revision 4.1, Small Form Factor Committee, July 6th 2009

[24] IEEE 802.1AE: Media Access Control (MAC) Security, IEEE 802.1 working group, September 25th 2015

[25] JESD79-3F/79-3-1: DDR3 SDRAM Standard

[26] JESD79-4: 3DS DDR4 SDRAM Standard

[27] JESD209-3C: Low Power Double Data Rate 3 SDRAM (LPDDR3)