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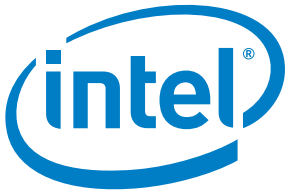
MaxLinear

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com



Intel® 10G PON Chipset

Intel® 10G PON Development Kit EASY PRX321 REF BOARD

PRX321 SFU Reference Board V1.2/V1.3

User's Manual

Hardware Description

Revision 1.0, 2018-09-18 Intel Confidential
Reference ID 617832

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Revision History

Current: **Revision 1.0, 2018-09-18**
Previous: **None**

Page	Major changes since previous revision

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Preface

This document describes the Intel® 10G PON Development Kit EASY PRX321 REF BOARD V1.2/V1.3, which is a demonstration platform to show the Intel® 10G PON Chipset PRX321 device used in a business 10G application.

The difference between the V1.2 and V1.3 boards relates to a fault concerning the I2C bus, where the signals have to be swapped at the SFP cage. This is implemented with extra wiring on the V1.2 board (see **Figure 2**) and will be resolved in the layout of the V1.3 board.

To simplify matters, the following synonym is used:

EASY PRX321 REF BOARD

Synonym used to refer to the Intel® 10G PON Development Kit EASY PRX321 REF BOARD V1.2/V1.3.

Organization of this Document

This document is organized as follows:

- **Chapter 1**, **Overview**
  Provides an overview of the features of the EASY PRX321 REF BOARD, including a block diagram.
- **Chapter 2**, **Power Supply**
  Describes the power supply generation on the EASY PRX321 REF BOARD and the power-up sequence.
- **Chapter 3**, **Pin Description**
  Describes the connectors on the EASY PRX321 REF BOARD, including detailed pinouts.
- **Chapter 4**, **Board Configuration**
  Describes how to configure and control the operating modes of the EASY PRX321 REF BOARD.
- **Chapter 5**, **Floorplans**
  Provides the top and bottom floorplans of the EASY PRX321 REF BOARD.
- **Literature References**

1 Overview

The top view of the EASY PRX321 REF BOARD is shown in **Figure 1** and the bottom view in **Figure 2**. The board is implemented as a 4-layer PCB and is used to demonstrate the PRX321 device, a member of the Intel® 10G PON Chipset.

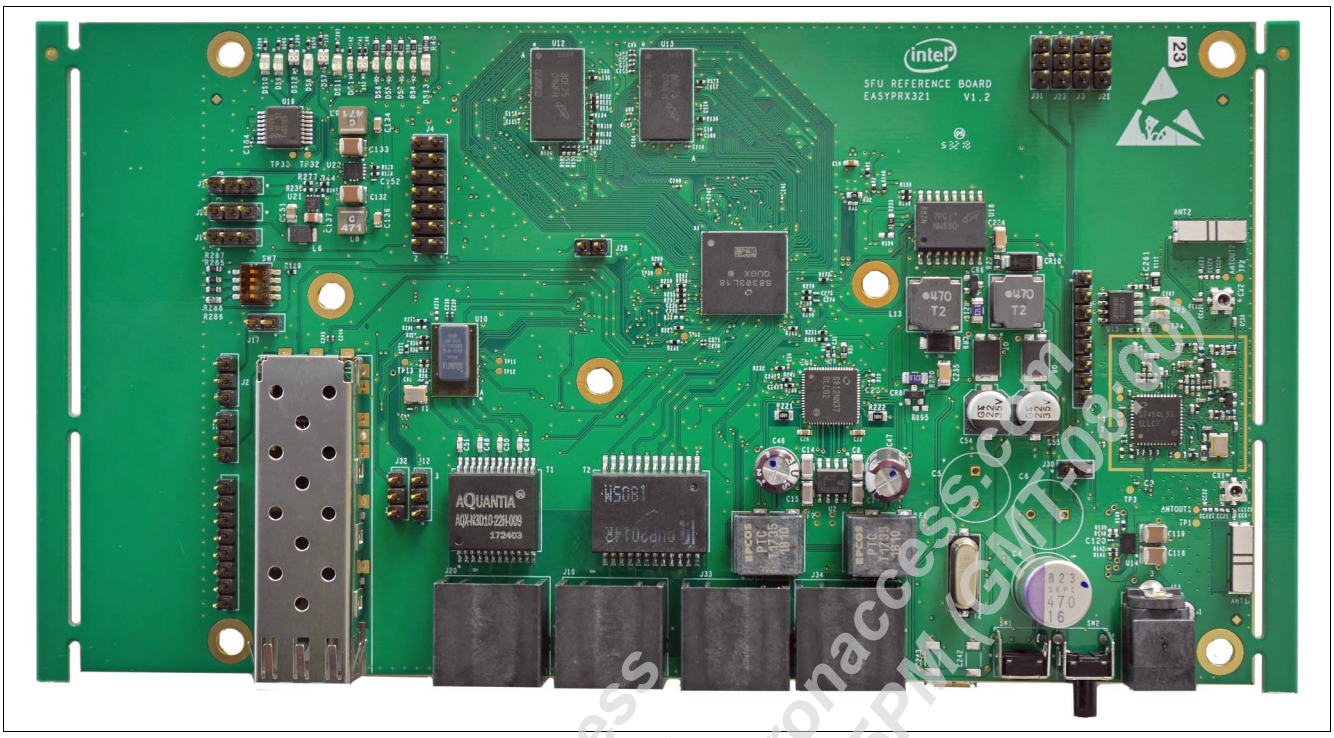


Figure 1 EASY PRX321 REF BOARD (Top View)

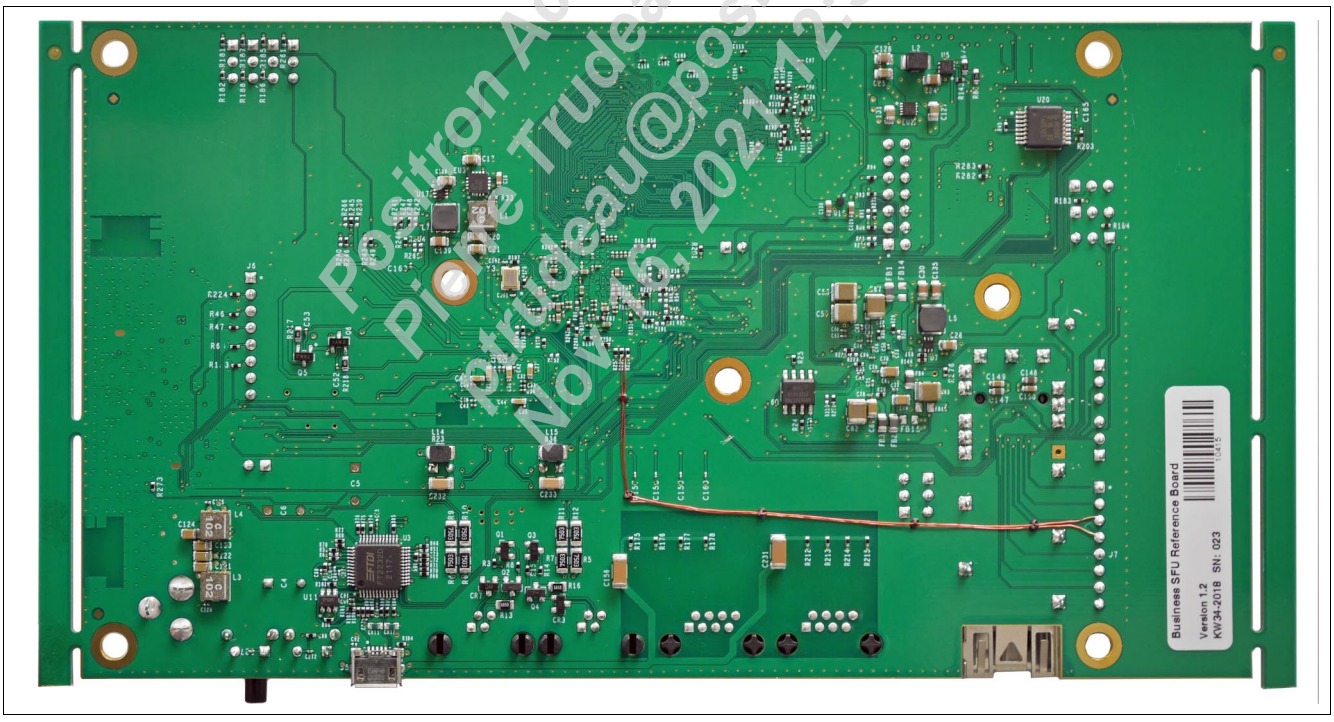


Figure 2 EASY PRX321 REF BOARD (Bottom View)

The system is powered with a single +12 VDC/3 A power supply connected to X1.

1.1 Block Diagram

As shown in **Figure 3**, and described in the sections below, the EASY PRX321 REF BOARD includes the following components.

- Intel® 10G PON Chipset PRX321
- Clocking
- DDR4 SDRAM Module
- Flash Memory
- PON Interface
- Internal 2.5G PHY
- External 10G PHY
- POTS supported by the Intel® SLIC for CPE SLC220 (EASY 42078-IBB12 board)
- DECT supported by the Intel® DECT Chipset DCL103
- LEDs
- Shift Register
- Debug and UART Interface
- DC/DC converter

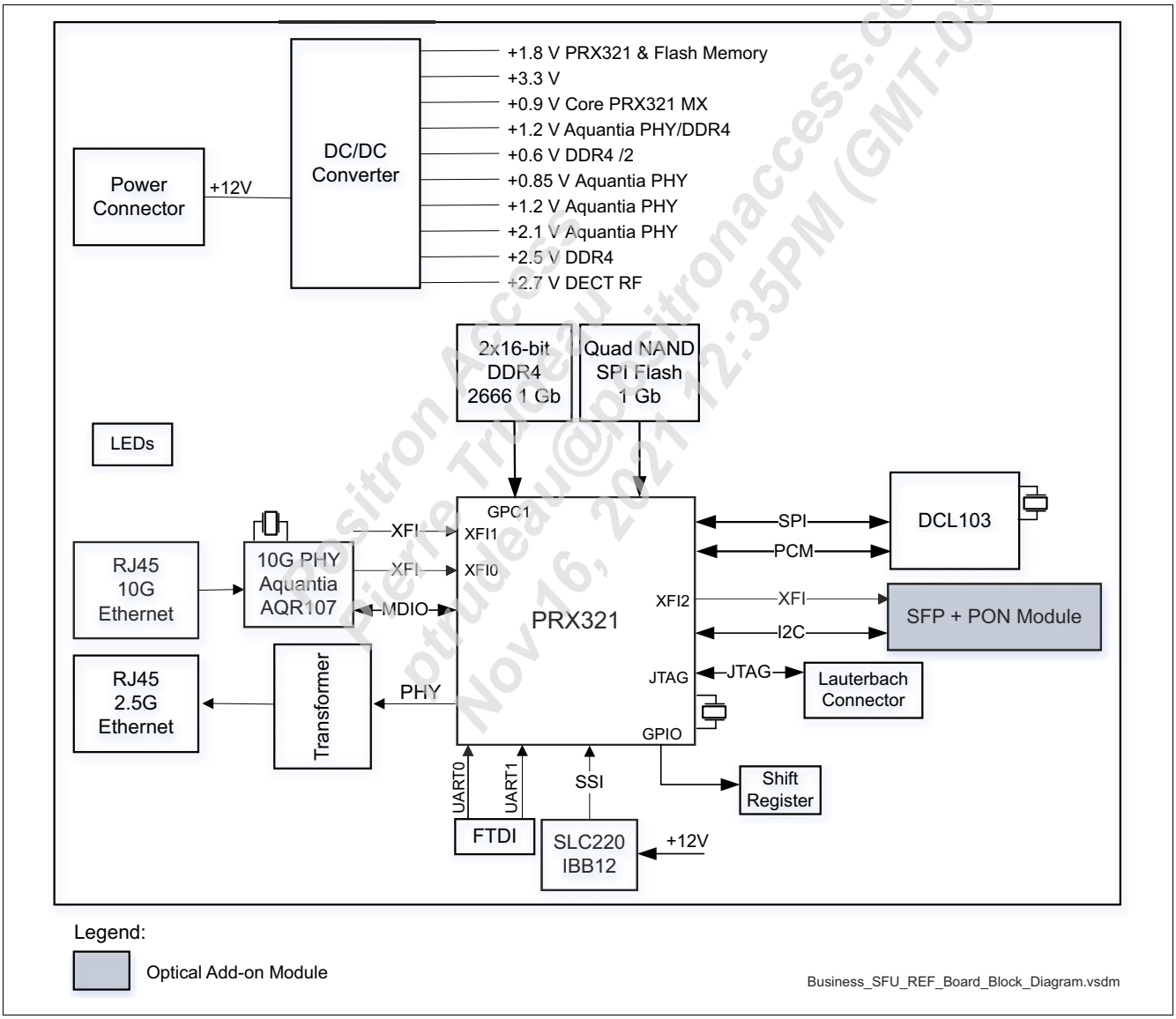


Figure 3 Block Diagram of the EASY PRX321 REF BOARD

1.2 Intel® 10G PON Chipset PRX321 Device

The Intel® 10G PON Chipset PRX321 device is the system controller of the board and controls and sets up all the system interfaces. The device provides interfaces for DDR SDRAMs (DDR3L, LPDDR3 or DDR4), flash memories in NAND and NOR technologies, one optical high speed interface (PON) and two XFI high speed interfaces for the connection of external high speed interfaces, e.g. 10G Ethernet and integrated 2.5G PHY. In addition, there is an SSI interface to connect POTS and PCM and SPI interfaces for connection to DECT.

There are LEDs connected directly to the device and to external devices. The PRX321 has 31 GPIOs offering special functions. In this application the system needs more GPIOs than this, therefore the PRX321 has three GPIOs that are used to control a shift register which extends the number of GPIOs. In this application the shift register is 16 bit. The GPIOs are described in **Table 1**.

Table 1 PRX321 **GPIO Functions**

GPIO	Name	Direction	Function	Connected to
0	SPI_SCK	O	SPI	Serial flash memory
1	SPI_CS_N	O	SPI	Serial flash memory
2	SPI_IO0	I/O	SPI	Serial flash memory
3	SPI_IO1	I/O	SPI	Serial flash memory
4	SPI_IO2	I/O	SPI	Serial flash memory
5	SPI_IO3	I/O	SPI	Serial flash memory
6	SSI_CLK	I	SLC220	SLIC_CLKO at TID0 connector, no pull-up/down
7	SSI_TX	O	SLC220	SLIC_RX at TID0 connector, no pull-up/down
8	SSI_RX	I	SLC220	SLIC_TX at TID0 connector, no pull-up/down
9	TDM_FSC	O	DECT	DECT, FSC PCM Bus
10	MDC0	O	SerDes I/F	Aquantia 10G PHY, data clock
11	MDIO	I/O	SerDes I/F	Aquantia 10G PHY, data signal
12	SPI1_CLK	O	DECT	DECT, SPI data clock
13	SPI1_MTSR	O	DECT	DECT, SPI MRST, pull-up
14	LED-SH		Shift Reg.	External shift register, data latch
15	LED_ST		Shift Reg.	External shift register, shift transmit
16	LED_D		Shift Reg.	External shift register, shift data
17	SPI_MRST	I	DECT	DECT, SPI MRST, pull-up
18	TDM_DCL	O	DECT	DCT, DCL PC, bus
19	SSI_CLKI	O	SLC220	SLIC CLKI at SLC220
20	LOS	I	PON	Loss of signal (SFP/XFP), pull-up
21	INT_N	I	DECT	DECT interrupt active low, pull-up
22	TxFAULT	I	PON	TxFAULT of SFP/XFP
23	TX_SD	I	PON	Transmitter signal detect of SFP
24	TDDM_DI	I	DECT	PCM TX of DECT, pull-up
25	TDM_DO	O	DECT	PCM RX of DECT, pull-up
26	I2C_SCL	O	PON	SFP/XFP cage, pull-up
27	I2C_SDA	I/O	PON	SFP/XFP cage, pull-up
28	DECT_CS_N[1)]	O	DECT	Chip select of DECT or LED on/off button, pull-up

Table 1 PRX321 **GPIO Functions** (cont'd)

GPIO	Name	Direction	Function	Connected to
29	DECT_CS	O	PON	–
30	UART1_RX[2)]	I	DEBUG/DECT	RS232 or DECT paging button, pull-up
31	UART1_TX[3)]	O	DEBUG/PON	RS232 or SFP 1588 ToD signal
OPT_TXEN	OPT_TXEN	O	PON	SFP/XFP cage

1) GPIO28 can be used for DECT or as LED on/off button.
2) GPIO30 is used for debugging or as DECT paging button when there is no debugging.
3) GPIO31 can be used for debugging or as ToD signal when there is no debugging.

1.3 Clocking

There is no central clocking unit available, but three separate crystals for the following parts of the system:

- Intel® 10G PON Chipset PRX321: 40 MHz crystal with ±30 ppm tolerance
- Intel® DECT Chipset DCL103: 20.736 MHz crystal
- Aquantia 10G GPHY: 50 MHz crystal

The SLC220 is clocked from the PRX321, generating its own internal clock from the SSI_CLK signal.

Each of the crystals operates in the fundamental mode and has two external capacitors.

1.4 DDR4 SDRAM

The EASY PRX321 REF BOARD is equipped with two DDR4 SDRAMs from Micron with 2667 Mtps (2 devices 256M x 16bit, each in single rank). Each device has a memory of 4 Gbytes, giving a total of 8 Gbytes. The ordering number for the Micron devices is MT40A512M16LY-075E:B (256M x 16, CL=19).

1.5 Flash Memory

A 2 Gbyte QUAD SPI NAND flash memory with a SOIC-16 (300 mil) footprint is used as the default on the EASY PRX321 REF BOARD. No socket is provided. It is also possible to use alternative flash memories that have the same footprint, with quad SPI, dual SPI or single SPI interfaces and in different memory sizes. EEPROMs or NOR flash memories can also be used and the voltage rail can be varied between 1.8 V and 3.3 V via mounting options (0 Ω resistors).

1.6 Optical Interface (PON)

The optical interface is fitted with an SFP cage to allow any optical module with the pinout described in **Chapter 3.4** to be connected. The power supply (+3.3 V) of the SFP is connected directly to the 3.3 V power rail and only decoupling capacitors are connected to the SFP power pins. The power rail cannot be switched on or off, and the rail is not filtered by inductors so that high currents are possible.

1.7 2.5G Ethernet Interface

A transformer and RJ-45 jack are connected to the internal 2.5G PHY to support a 2.5G Ethernet interface.

1.8 10G Ethernet Interface

The high speed interface signal SERDES 0 is connected to the Aquantia PHY (AQR-107) to support a 10G Ethernet interface. The PHY has an external transformer, a RJ-45 socket, an SPI flash memory and a crystal.

The EASY PRX321 REF BOARD can alternatively be used with the Aquantia AQR-113 instead. All the necessary mounting options are available, however, it would then not be possible to remount the system with the other PHY.

1.9 Analog Telephone Lines (POTS)

There are two analog POTS telephone lines available, which are supported by the SLC220. Each line has its own Inverted Buck Boost Converter at 12 V (IBB12). There is a built-in option to allow a single DC/DC converter to be used for both analog telephone lines with a lower ringing voltage and lower ringer loads. This mode is called Combined Inverted Buck Boost Converter (CIBB12). The +1.5 V supply for the SLC220 is generated by the SLC220 itself in linear mode. Both telephone lines have on-board K.20 protection (PTC and thyristor). Two telephone sets can be connected to the board via two RJ-11 jacks.

1.10 DECT Interface

The DECT interface is realized with the Intel® DECT Chipset DCL103 and two antennas. The DECT part is controlled by the SPI interface. The chip select signal (DECT_CS_N) is not a real SPI chip select. It is connected to the port P0.0 of the DCL103 and controls the flow (RX and TX).

1.11 Shift Register

A shift register is implemented to extend the number of GPIO output signals. The PRX321 supports a shift register with a maximum length of 32 bits. In the case of this EASY PRX321 REF BOARD, the shift register only needs 16 bits. The first bit shifted out of the PRX321 is bit 0. The shift register bits are described in Table 2.

Table 2 Shift Register Bits

Bit	IC	Pin	Function
0	U19	7	NU (connected to test pad TP32)
1	U19	6	NU (connected to test pad TP33)
2	U19	5	PHY_LED0 (dual LED DS7)
3	U19	4	PHY_LED1 (dual LED DS7)
4	U19	3	PHY_LED2 (DS8)
5	U19	2	LED_PON0 (dual LED DS12)
6	U19	1	LED_PON1 (dual LED DS12)
7	U19	15	LED_VOICE0 (DS9)
8	U20	7	LED_VOICE1 (DS10)
9	U20	6	LED_DECT (DS11)
10	U20	5	SFP RATE_SEL
11	U20	4	NC
12	U20	3	NC
13	U20	2	AQUANTIA RES_N
14	U20	1	DECT RES_N
15	U20	15	SLC220 RES_N

1.12 LEDs

There are 8 single color LEDs and 2 dual color LEDs on the board.

- 1 LED (green) shows active power supply (+3.3 V)

The following LEDs are connected via the shift register:

- 1 dual color LED (red/green) for 2.5G Ethernet
- 1 LED (green) for link status of 2.5G Ethernet
- 2 LEDs for voice
- 1 LED for DECT
- 1 dual color LED for PON (green/red)

The Aquantia PHY device controls the following LEDs:

- 2 LEDs (red/green) for Aquantia PHY
- 1 LED (green) of link status

There are no LEDs for the interrupt signals.

1.13 Debug and UART

The UART0 and UART1 interfaces of the PRX321 are connected to a FTDI chip such that both UART interfaces can be supported via one USB interface to a PC. The UART0 interface uses channel 0 of the USB and UART1 uses channel 1. A micro USB plug is placed on the board to allow a PC to be connected.

2 Power Supply

The system is powered from one external AC/DC wall power supply with a 12 VDC/1 A output rail and connected to X2. All the voltage rails are generated from this input. All PRX321 power rails, DDR4 SDRAM and external PHY rails are generated from the +3.3 V rail for good efficiency. The block diagram is shown **Figure 4**.

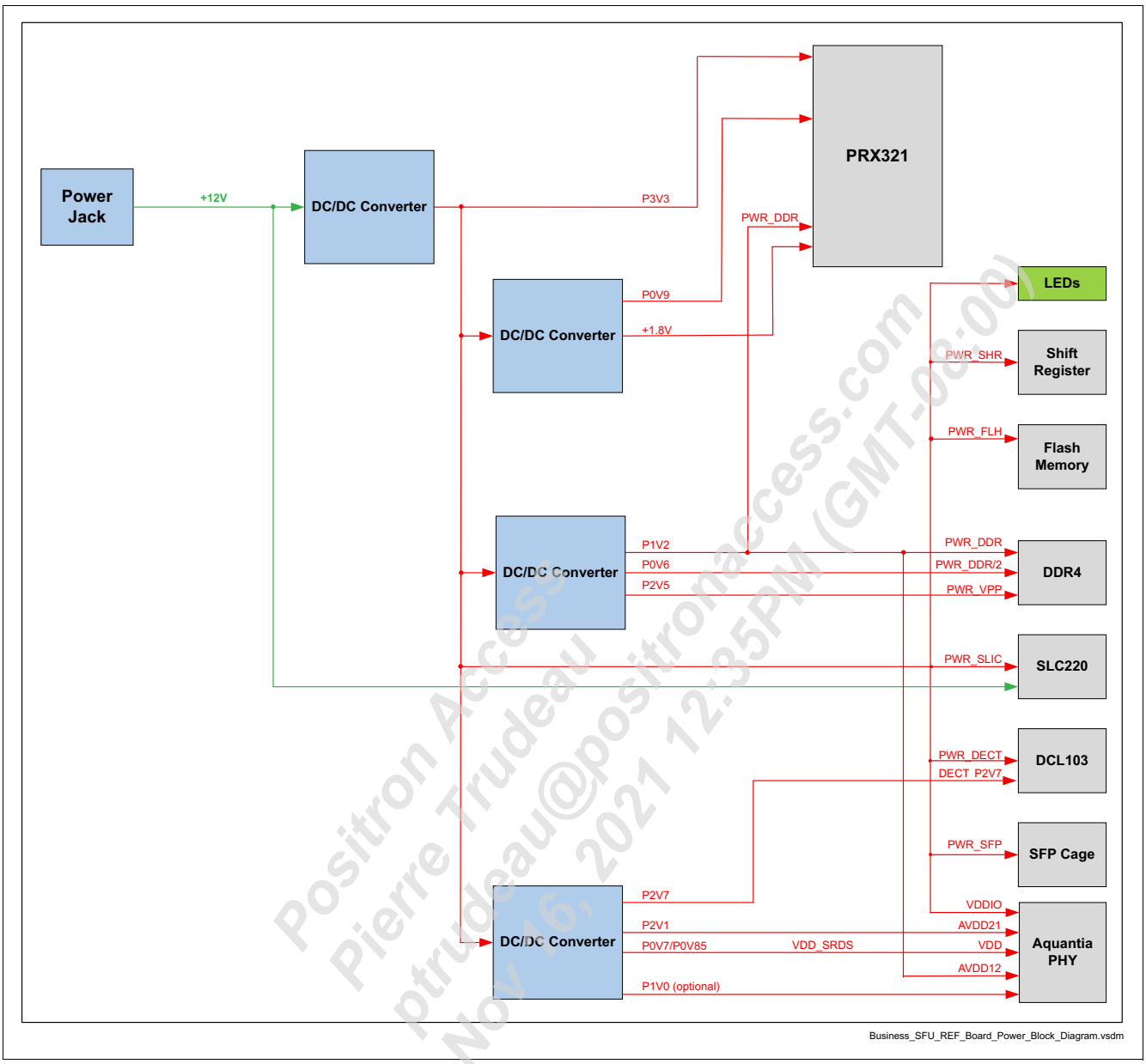


Figure 4 Block Diagram of the EASY PRX321 REF BOARD Power Generation

The built-in power-on sequence is shown **Figure 5**. It guarantees that the 0.85 V power rail is enabled 10 ms after the 3.3 V rail is stable.

The DC/DC converters of the SLIC use the external 12 V supply.

The system also supports a dying gasp function, with a voltage divider defining the activation level. The blocking capacitance of the 3.3 V rail is calculated to have enough energy to send the dying gasp message to the uplink device.

The system use the DC/DC converters as defined in **Table 3**.

Table 3 DC/DC Converter Specification

Voltage Rail [V]	Input Voltage [V]	Max. Output Current [mA]	DC/DC Type	Sequence
+3.3	+12	5800	TI TPS62184	1
+1.8	+3.3	800	TI TLV62568	2
+0.9	+3.3	3600	TI TLV62095	4
+1.2	+3.3	1200	TI TLV62085	3
+0.6	+3.3	500	TI TPS51206	3
+2.5	+3.3	4	TI LP5900TL-2.5	3
+2.7	+3.3	650	TI TLV62568	2
+2.0/+2.1[1)]	+3.3	460	TI TLV62568	2
+0.7/+0.85[1)]	+3.3	3700	TI TPS624580	2
+1.5	+3.3	40	SLC220	2
+1.0[1)]	+3.3	1200	TLV62085	2

1) The +2.0 V, +0.7 V and 1.0 V rails are options for the Aquantia PHY AQR-113.

The power-up sequence is set as shown in **Figure 5**.

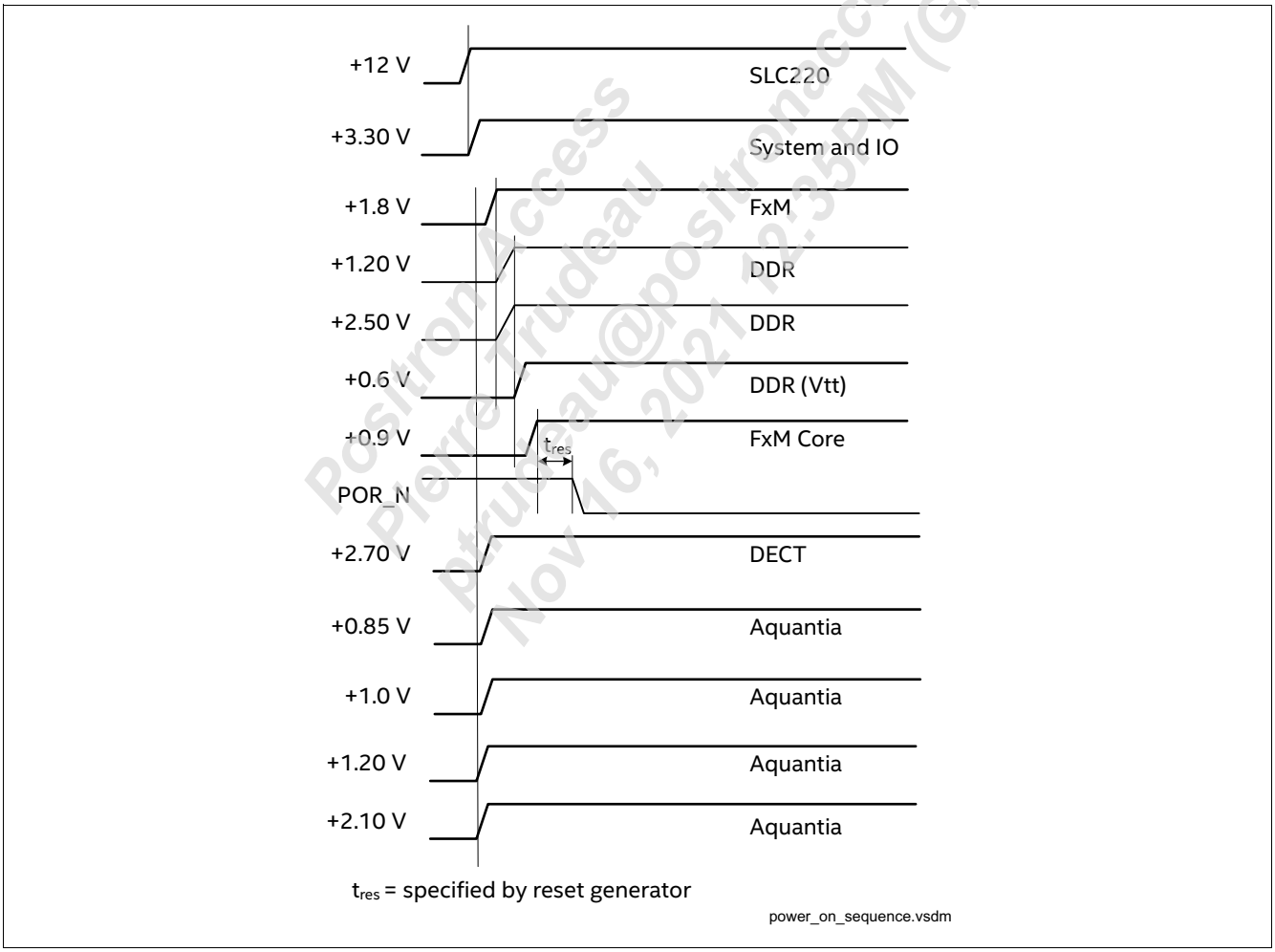


Figure 5 Power-on Sequence

3 Pin Description

This chapter provides a description of all the connectors available on the EASY PRX321 REF BOARD including the pinout descriptions for the test headers.

3.1 Power Supply Socket (J11)

The +12 V power supply is connected to the board via the power socket J11.

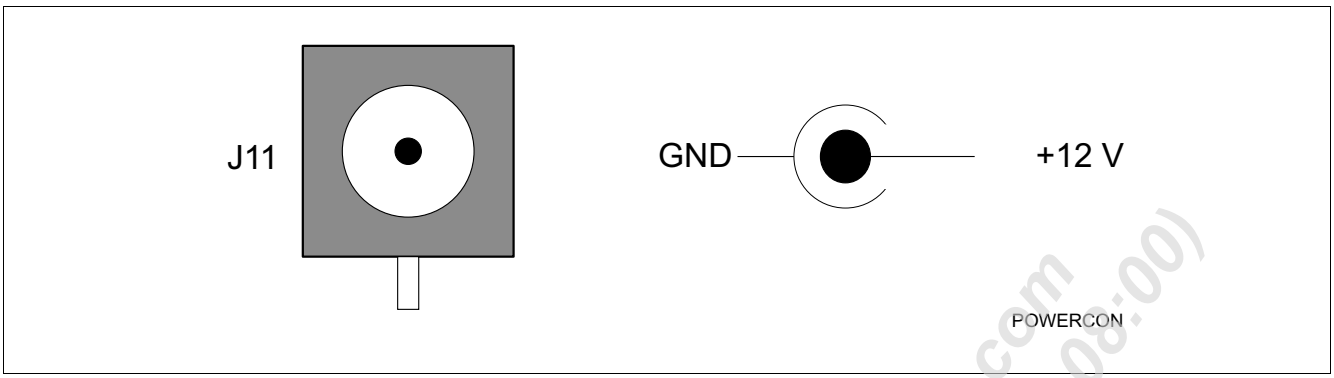


Figure 6 Power Socket (J11)

3.2 RJ-45 2.5G and 10G Ethernet Jacks (J10, J20)

There are two Ethernet interfaces on the board. The internal interface of the PRX321 is a 2.5G Ethernet interface and the Aquantia PHY has a 10G Ethernet interface. Both jacks have the same pinout.

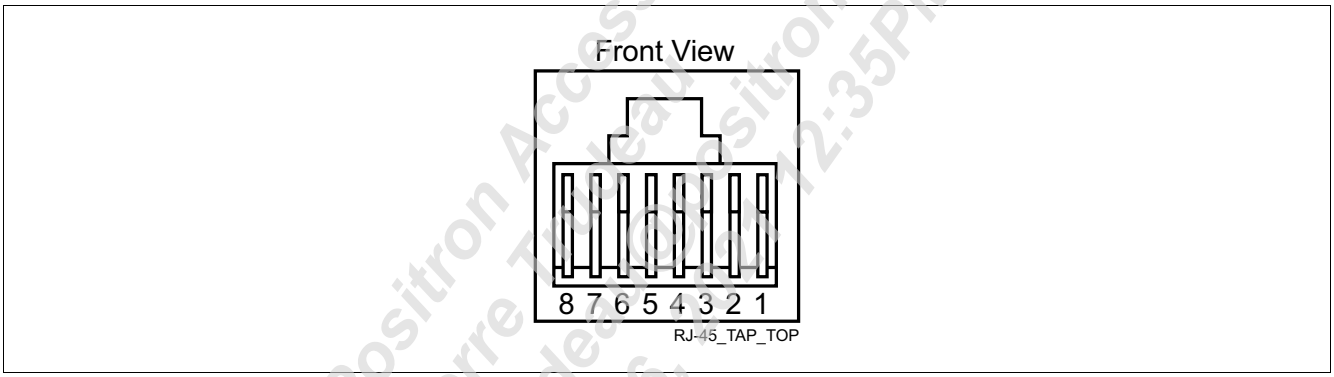


Figure 7 RJ-45 Ethernet Jacks (J10, J20)

Table 4 RJ-45 Ethernet Jacks (J10, J20)

Pin	Use	Function
1	I/O	MX_A+
2	I/O	MX_A-
3	I/O	MX_B+
4	I/O	MX_C+
5	I/O	MX_C-
6	I/O	MX_B-
7	I/O	MX_D+
8	I/O	MX_D-

3.3 RJ-11 Analog Telephone Jacks (J33, J34)

The RJ-11 jacks on the EASY PRX321 REF BOARD allow phone sets to be connected to the analog voice channels (lines), J33 for channel B and J34 for channel A.

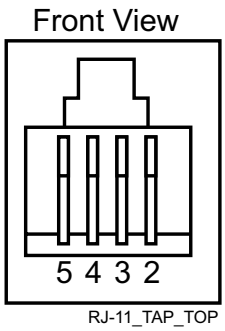


Figure 8 RJ-11 Analog Telephone Jacks (J33, J34)

Table 5 RJ-11 Analog Telephone Jacks (J33, J34)

Pin	Use	Function
1	–	–
2	I/O	RING
3	I/O	TIP
4	–	–

3.4 SFP Connector Cage (J9)

The optical interface (PON) of the PRX321 is connected to an SFP cage.

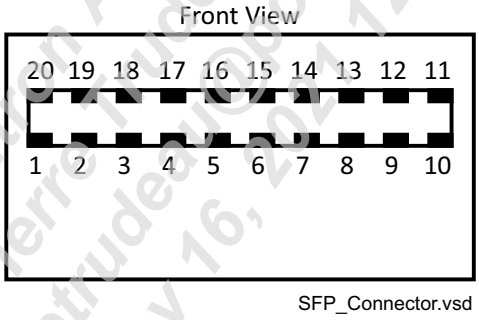


Figure 9 SFP Connector Cage J9 (Front View)

Table 6 SFP Connector Cage (J9)

Pin	Use	Function	Connected to
1	I/O	GND	–
2	I/O	TXFAULT	PRX321 GPIO22
3	I/O	TXDIS	PRX321 OPT_TXEN
4	I/O	I2C_SDA	PRX321 GPIO26
5	I/O	I2C_SCL	PRX321 GPIO27
6	I/O	PRES	Header J33 pin 5
7	I/O	RATE_SEL	Shift register bit 9 via option resistor or GPIO28
8	I/O	LOS	PRX321 GPIO20
9	I/O	GND/PPS	J13 to select PRX321 GPIO24, GND or +3.3 V
10	I/O	GND	–
11	I/O	GND	–
12	I/O	RX_N	PRX321 P2_RXN
13	I/O	RX_P	PRX321 P2_RXP
14	I/O	GND	–
15	I/O	+3.3 V	–
16	I/O	+3.3 V	–
17	I/O	GND	–
18	I/O	TX_P	PRX321 P2_TXP
19	I/O	TX_N	PRX321 P2_TXN
20	I/O	GND	–

3.5 USB Debug Connector (J5)

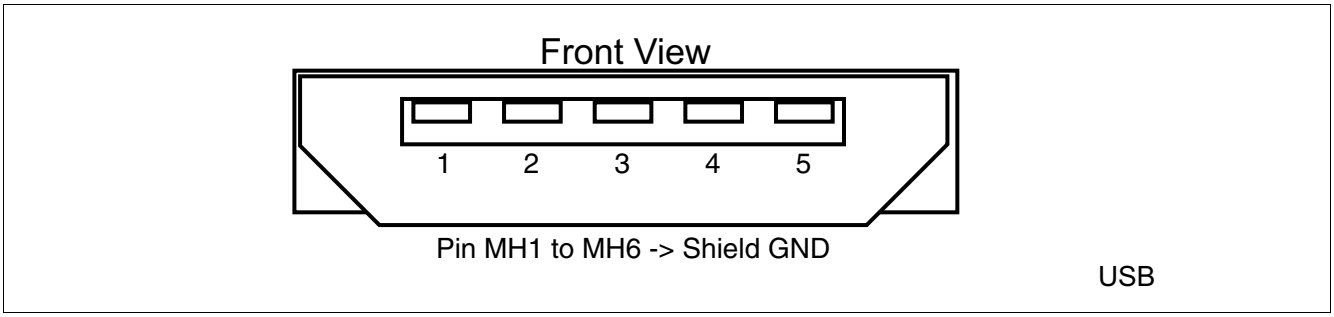
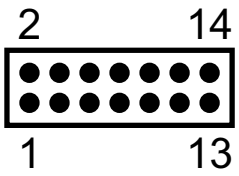


Figure 10 USB Debug Connector J5 (Top View)

Table 7 USB Debug Connector (J5)

Pin	Use	Function
1	I/O	VBUS +5 V
2	I/O	D-
3	I/O	D+
4	–	–
5	I/O	GND
MH1	I/O	Shield GND
MH2	I/O	Shield GND
MH3	I/O	Shield GND
MH4	I/O	Shield GND
MH5	I/O	Shield GND
MH6	I/O	Shield GND

3.6 Lauterbach Debug Connector (J4)



DEBUG_CON

Figure 11 Lauterbach Debug Connector (J4)

Table 8 Lauterbach Debug Connector (J4)

Pin	Use	Function
1	I/O	RST_N
2	–	Not connected
3	O	TDI
4	I/O	GND
5	I	TDO
6	I/O	GND
7	I	TMS
8	I/O	GND
9	I	TCK
10	I/O	GND
11	I/O	POR_N
12	–	Not connected
13	I/O	BREAK (default not connected)
14	I/O	+3.3 V

3.7 Headers, Jumpers and Test Points

The EASY PRX321 REF BOARD provides test headers to allow signals to be measured, jumpers to select signals and their functions, and test points to allow special access to the signals, except for the high speed signals.

3.7.1 Test Headers

The test headers are used to measure signals at various components, such as the optical modules, Aquantia 10G Interface, reset signals and the PRX321 fan connection.

3.7.1.1 PON Interface Headers (J7, J17)

The signals at the SFP cage, except for the high speed signals, are accessible via test headers J7 and J17.

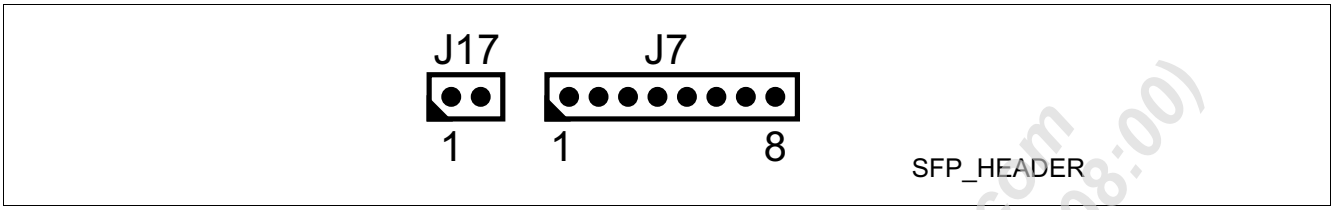


Figure 12 SFP Test Header (J7, J17)

Table 9 SFP Test Header (J7)

Pin	Function
1	TxFAULT
2	TXDIS
3	I2C_SCL
4	I2C_SDA
5	RES
6	RATE_SEL
7	LOS
8	GND

Table 10 SFP Test Header (J17)

Pin	Function
1	Pin 9 of SFP cage
2	GND

3.7.1.2 Additional Header

Additional headers are used for various test signals for serial interfaces, reset signals, the shift register and the JTAG interface.

Table 11 PRX321 Test Header (J28)

Pin	Function
1	POR_N of PRX321
2	GND

Table 12 Shift Register Test Header (J29)

Pin	Function
1	DECT_RES_N (DECT active low reset)
2	AQR_RES_N (Aquantia PHY active low reset)
3	SSI_RES_N (SLC220 active low reset)

Table 13 PRX321 Fan Header (J30)

Pin	Function
1	+12 V
2	GND

Table 14 Aquantia PHY Test Header (J12)

Pin	Function
1	AQR_MDC
2	AQR_MDIO
3	GND

Table 15 Aquantia PHY SM Bus Test Header (J32)

Pin	Function
1	SM Bus clock
2	SM Bus DAT
3	GND

3.7.2 Jumpers

Jumpers are provided on the EASY PRX321 REF BOARD to select the boot modes and the optical module pin functions.

3.7.2.1 Boot Mode, Flash Power Rail, Endianess and JTAG Mode Setting Jumpers

The boot mode of the PRX321 can be selected using 4 jumpers, and the power rail itself is selected via 4 option resistors. Other mode settings for Endianess, JTAG and flash power mode are also set using jumpers.

In the tables describing the jumper settings, 0 means a connection between pin 1 and pin 2, 1 means a connection between pin 2 and pin 3.

Table 16 Boot Mode Setting

J3	J23	J22	J21	Boot Mode
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	UART0 XMODEM
0	0	1	1	SPI NAND
0	1	0	0	Legacy UART0
0	1	0	1	NOR or EEPROM at SPI
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	QSPI (Single Bit NOR FLASH)
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	QSPI (Quad BIT NOR Flash)
1	1	0	0	QSPI (Quad Bit NAND Flash)
1	1	0	1	QSPI (Single Bit NAND Flash)
1	1	1	0	Reserved
1	1	1	1	Reserved

Endian, debug and flash power modes can only be selected via mounting options. No jumpers are available.

Table 17 Endian Mode Setting

Endianess Mode	R190	R152
Little Endian	Mounted	Not mounted
Big Endian	Not mounted	Mounted

Table 18 JTAG Mode Setting

JTAG Mode	R192	R191
Debug mode	Mounted	Not mounted
Boundary Scan mode	Not mounted	Mounted

Table 19 Flash Power Mode Setting

Flash Power Mode	R194	R193
+1.8 V Flash Power Supply	Mounted	Not mounted
+3.3 V Flash Power Supply	Not mounted	Mounted

The GPIO output voltage must also be set at the pin VCC_IO_2 of the PRX321 with R196, R233.

3.7.2.2 Jumpers to Select the Cage Signals

Jumpers are used to select the optical module signals for interrupt, TxFault/ToD and RSEL_INT.

Table 20 Jumpers to Select the Cage Signals

Jumper	Function Selection
J1	GPIO28 is connected to interrupt of AQR-107 or the interrupt of the cage (via J2)
J2	SFP_RATE_SEL or XFP_INT is connected to J1 or to the shift register
J31	TxFAULT of the cage is connected to OPT_TxFAULT or UART1_TX

3.7.3 Test Points

Test points are placed at all device pins that are not connected, and to allow signals to be selected or measured.

3.7.3.1 Test Points for DECT

The DECT part has test points to measure the not connected signals from the DCL103 device.

Table 21 DECT Test Points

Test Point	Signal
TP1	GND
TP2	GND
TP3	GND
TP4	GND
TP5	GND
TP6	P1_5 (pin 41) of DCL103 chip
TP7	P1_4 (pin 40) of DCL103 chip
TP8	P1_3 (pin 38) of DCL103 chip
TP9	P1_2 (pin 37) of DCL103 chip
TP10	P1_0 (pin 13) of DCL103 chip

Table 22 Aquantia Signal Test Points

Test Point	Signal
TP11	CLK_1588_P
TP12	CLK_1588_N
TP13	CLKO_50M_A

There is no test header for the SFP and XFP high speed signals as these signals could be affected by the pins of the header. Instead, there are very small vias that allow access, where a small wire can be soldered onto the board to allow connection if required.

Table 23 PRX321 Test Points

Testpoint	Function
TP30	HRST output of PRX321
TP31	GPIO23 input or output

4 Board Configuration

This chapter describes how to configure the EASY PRX321 REF BOARD system, including the jumpers and mounting options.

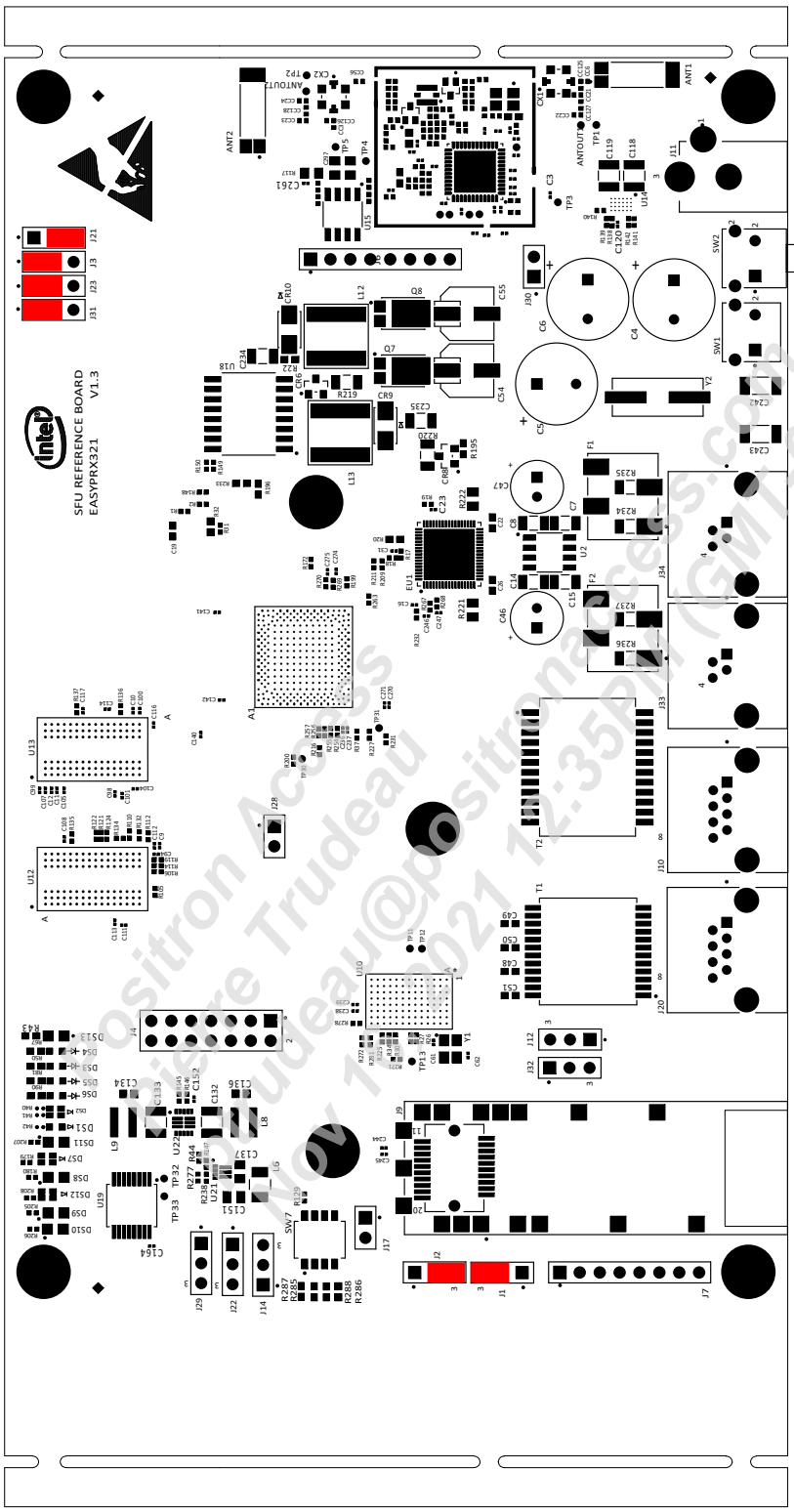


Figure 13 Default Jumper and Mounting Option Selection (Top View)

4.1 Power Supply Selection for Flash

The system and the PRX321 support serial NAND and NOR flash memories with two different voltage rails. The interface supports serial NAND, NOR or EEPROM with single bit, dual or quad SPI mode. The setting of the boot mode is described in **Chapter 4.2**.

The voltage rail can be +1.8 V or +3.3 V. The voltage rail is selected via R196 and R233; the jumper J27 selects the same information for the PRX321 to use the correct signal driving.

Table 24 Power Supply Setting for Flash Memory

Power Rail	J27	R196	R233	Default
+1.8 V	pin 2 - pin 3 connected	Mounted	Not mounted	–
+3.3 V	pin 1 - pin 2 connected	Not mounted	Mounted	Default mode

4.2 Boot Mode Selection

The boot mode settings select the SPI mode, the voltage rail for the flash memory, the flash memory type, the endianness mode and the JTAG interface mode. The possible modes and the jumper settings are described in **Chapter 3.7.2.1**.

4.3 PON Module Selection and Aquantia PHY Interrupt

A large number of different modules are available for SFP and the signals on the pins can have different functions. Therefore it is necessary to compare the module data sheet with the tables in **Chapter 3.7.1.1** and **Chapter 3.7.2.2** and the possible mounting options shown in **Table 25**.

The SFP signal RATE_SEL is connected to the shift register or to GPIO28. The selection is configured using jumpers J1 and J2.

Table 25 Signal Configuration for SFP_RATE_SEL and XFP_INT

J1	J2	Cage	GPIO28	Shift Register	Default
pin 2 - pin 3 connected	pin 2 - pin 3 connected	SFP is plugged in	GPIO28 controls RATE_SEL	Not used	–
pin 1 - pin 2 connected	pin 1 - pin 2 connected	SFP is plugged in	Interrupt input from Aquantia	RATE_SEL to SFP	Default mode

Pin 9 of the SFP connector is only connected to J17, which can be used for measurements. Alternatively, the pin can be connected to GND via a jumper.

5 Floorplans

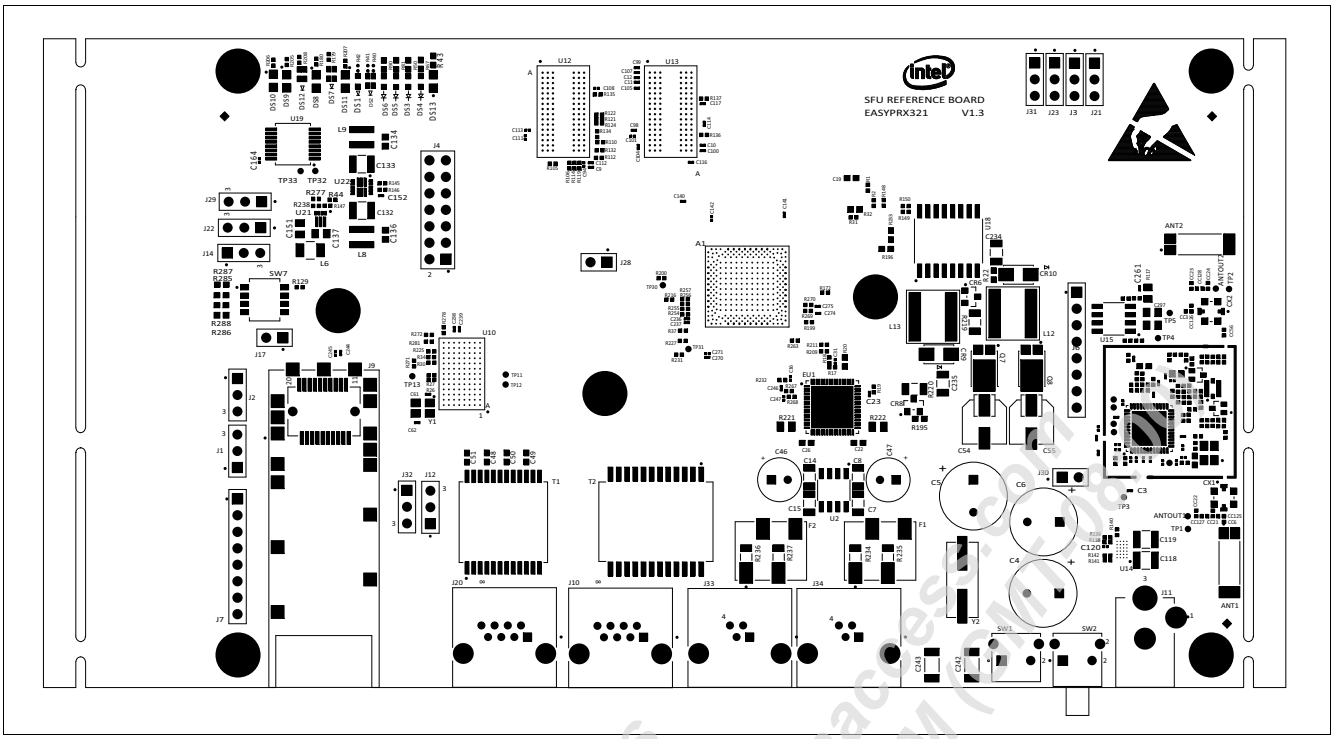


Figure 14 Top View of EASY PRX321 REF BOARD

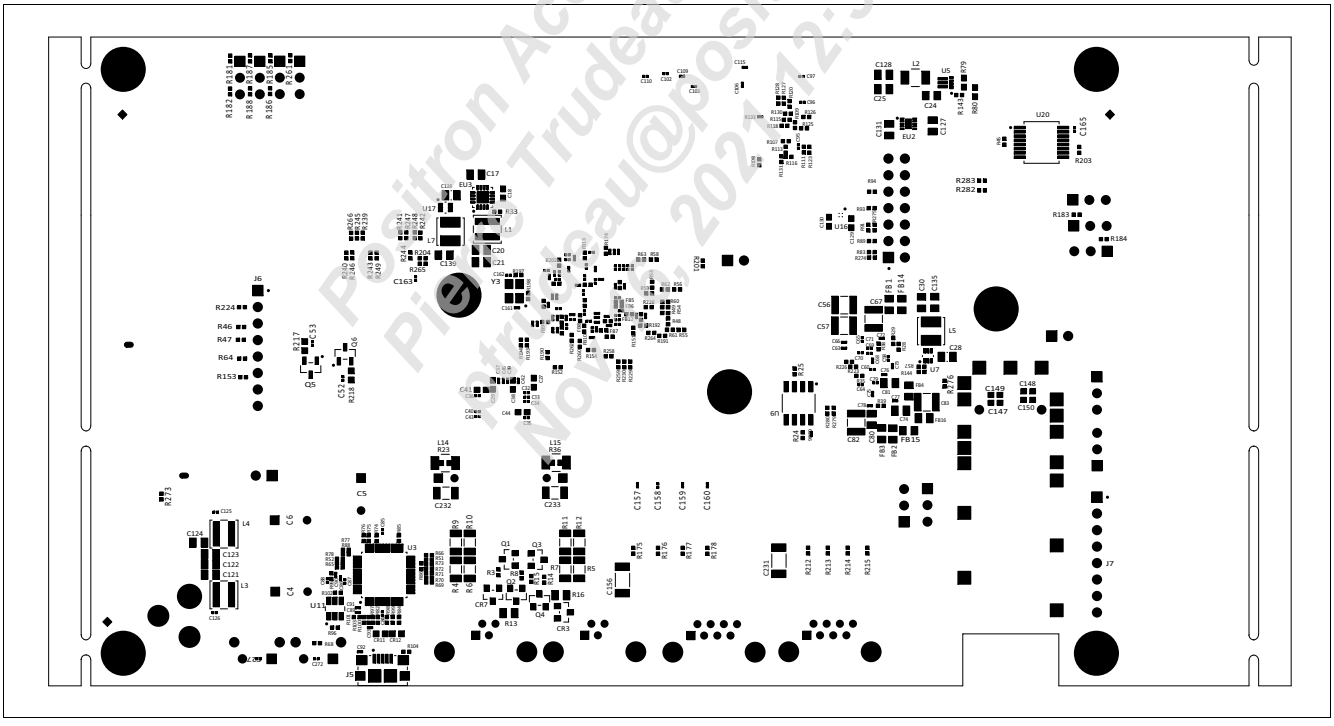


Figure 15 Bottom View of EASY PRX321 REF BOARD

Literature References

[1] Intel® 10G PON Chipset PRX321 (PRX321A1BI) Preliminary Data Sheet Rev. 1.0

Attention: Please refer to the latest revisions of the documents.